



TXW818 Datasheet



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Revision History

Date	Version	Revision Notes	Reviser
2024-04-26	V1.2	Updated product characteristics	TX
2024-01-16	V1.1	Supplementary Electrical Parameters Suggested Operating Conditions Description	TX
2023-12-26	V1.0	Initial version, future updates are subject to change without notice, please contact our sales staff for the latest version.	TX



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1. Product Overview

1.1. Description

The TXW818 is a low-power, high-performance, highly integrated 2.4GHz Wi-Fi and small wireless multi-mode IoT SOC chip. It integrates IEEE 802.11 b/g/n baseband and RF circuits, including a power amplifier (PA), low noise amplifier (LNA), RF balun, antenna switch, and power management module.

The TXW818 Wi-Fi baseband implements Orthogonal Frequency Division Multiplexing (OFDM) technology, compatible with Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) technologies, supporting the IEEE 802.11 b/g/n protocol. It supports a standard bandwidth of 20MHz and narrow bandwidths of 5MHz/10MHz, providing a maximum physical layer rate of 72.2Mbit/s.

The TXW818 chip integrates a high-performance 32-bit microprocessor with built-in MJPEG (supporting VGA/720P) and offers a rich set of peripheral interfaces, including DVP, LCD, USB2.0 High Speed Host/Device, SDMMC Host, SDIO2.0 Slave, RMI MAC, SPI Master & Device, UART, IIC, IIS, PDM, IR Send/Receive, PWM, GPIO, and standard and audio ADC/DACs. It supports running programs on SPI Flash, RTOS, and third-party components, and comes with an open and easy-to-use development and debugging environment.

The TXW818 series includes multiple models available in the mainstream QFN68 package form. Depending on the packaging form, the peripheral resource configuration of the devices varies, with some packages supporting built-in PSRAM and Flash.

Application :

- Wireless audio & video + display applications
- Kids' camera
- Smart door locks

1.2. Features

- **Wi-Fi MAC & PHY**
 - Supports IEEE 802.11 b/g/n standards
 - Supports 1T1R mode with data rates up to 72.2Mbps
 - Excellent transmission power and reception sensitivity
 - Built-in PA, LNA, and RF switch
 - Supports STA, AP, AP+STA (relay), STA+STA functions
 - Frame aggregation (TX/RX A-MPDU, RX A-MSDU)
 - Supports RX STBC (Space Time Block Coding)
 - Supports WPA/WPA2/WPA3

- **BLE**
 - Supports fast Bluetooth network configuration
 - Supports Wi-Fi/BLE PTA coexistence

- **Video**
 - Supports video data sources via DVP, UVC, SPI camera input
 - One MJPEG encoder, supporting a maximum resolution of 1920*1080 @ 30fps
 - One MJPEG codec, supporting a maximum resolution of 1920*1080 @ 30fps
 - Supports time watermark, colorful photo frame, motion detection, and optical flow algorithm hardware acceleration

- **Audio**
 - Supports high-performance single-ended and differential analog mic inputs with built-in PGA
 - One delta-sigma audio ADC
 - One delta-sigma audio DAC
 - Supports sampling rates of 8/11.025/12/16/22.05/24/32/44.1/48 KHz

- **LCD**
 - Supports RGB interface, MCU8080 interface, and MCU6800 interface LCD displays
 - Supports image scaling, 90/180/270-degree rotation, horizontal and vertical mirroring
 - Supports image OSD, Alpha Blending
 - Supports CCM, Gamma correction, saturation, and contrast adjustment functions
 - Supports display resolution of 1280x720

- **MCU**
 - CK803 CPU, maximum clock speed 240MHz
 - 272KB SRAM
 - Supports various external frequency crystal oscillators and shared crystal

-
- oscillator input with the system main control chip
 - Supports RTC
 - Supports 32KHz crystal oscillator
 - 17 timers
 - One 32-bit timer in the always-on domain
 - Four 16-bit low-power mode timers supporting hardware low-power breathing light function
 - Eight 32-bit timers
 - Two 16-bit timers supporting IR transmission/reception and LED strip drive
 - One 24-bit system tick timer
 - One RTCC timer
 - Supports ULP and LP low-power modes with ULP mode current <math><28\mu\text{A}</math>@25° C, and multiple IO wake-up support
 - Built-in temperature sensor
 - Built-in LVD detection
 - Built-in watchdog
 - Built-in DC-DC power management module
 - Built-in multi-output LDO with output voltage range 1.8~3.3V
 - 48-bit unique chip ID (UID)
 - **Peripherals**
 - 47 programmable GPIOs, support edge or level triggered interrupts
 - 1 12-bit ADC, can be multiplexed as DAC
 - 1 12-bit analog comparator
 - 1 QSPI, support external SPI FLASH and PSRAM
 - 1 CMOS Sensor 8-bit DVP, support up to 120MHz interface
 - 1 Motion JPEG encoder
 - 1 Motion JPEG decoder
 - 1 LCD
 - 2 I2S/PCM
 - 1 PDM
 - 1 SDIO2.0 High Speed Device
 - 1 SD Host Controller
 - 1 USB2.0 High Speed Device/Host
 - 3 SPI interfaces Master/Slave (2 configurable as IIC Master/Slave)
 - 3 UART interfaces (1 supports flow control and RS485)
 - 2 infrared transmitters (1 supports IrDA) and multiple receivers
 - 14 PWM outputs (multiplexed with timer), including 4 independent 16-bit PWM, support low power mode PWM
 - **Boot Interfaces**
 - SDIO2.0 Device、USB2.0 Device、SPI Slave、UART

➤ SPI FLASH

● **Data Security**

- Support for AES 128/192/256 ECB/CBC/CTR encryption and decryption
- Support for SHA256
- Support for 5/7/8/16/32-bit CRC checking
- Support for SPI Flash firmware encryption protection
- TRNG (True Random Number Generator)

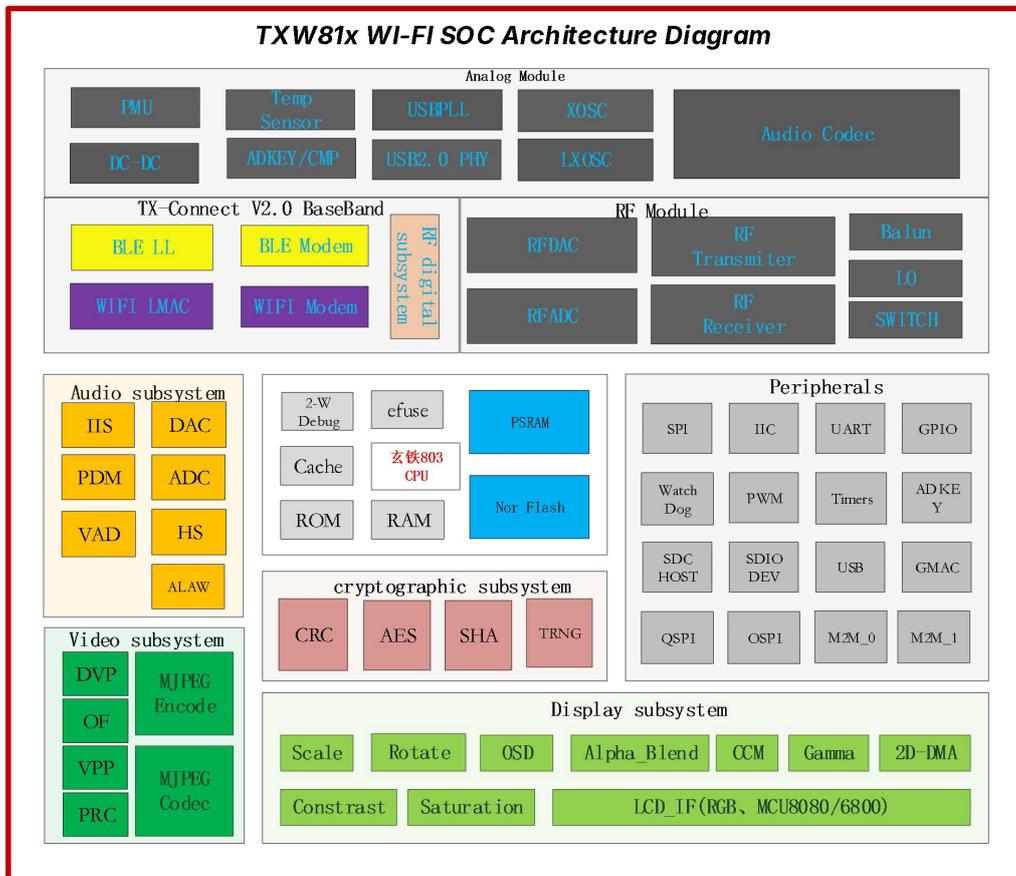
● **Package**

- QFN68 7x7 package

● **Temperature Range**

- -40° C to 85° C

1.3. Function Block Diagram



Note: Nor Flash and PSRAM are built-in in part of the chip package.

1.4. Pin Assignment

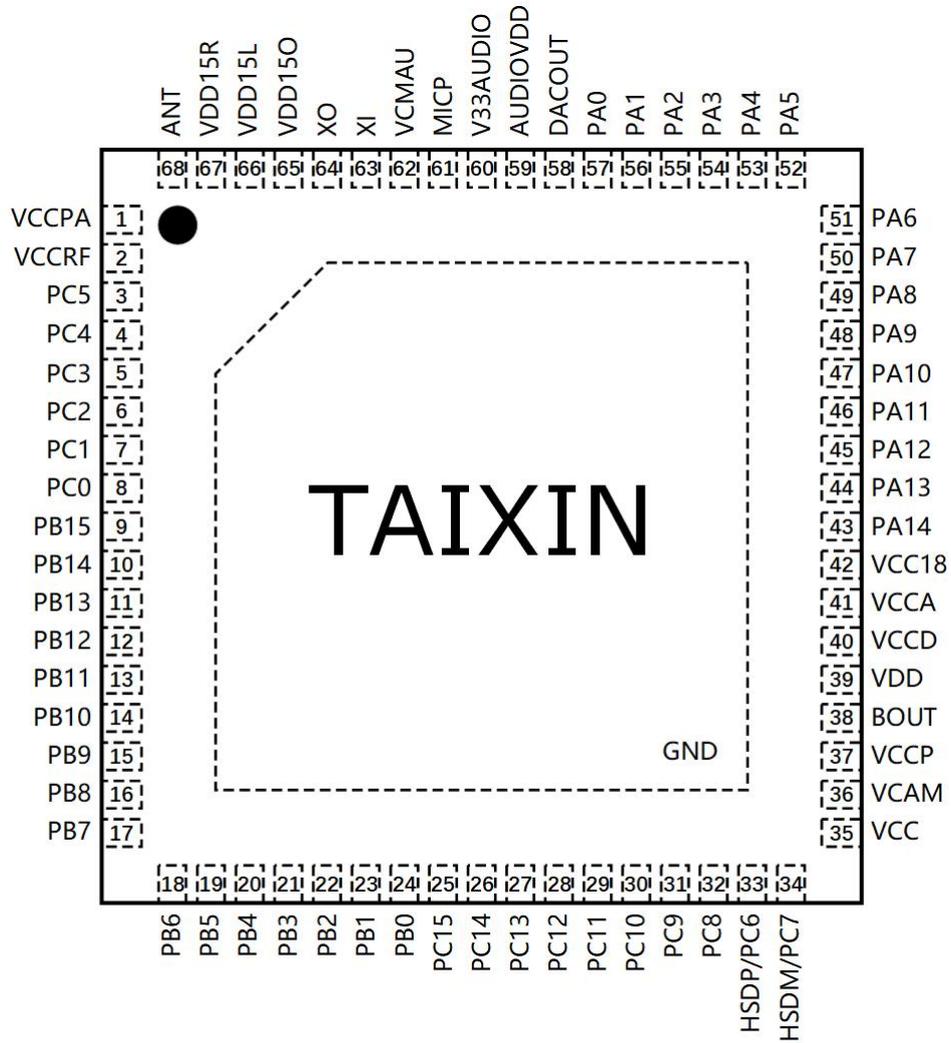


Figure 1-4-1 TXW818-C0xL QFN68 Package Pinout

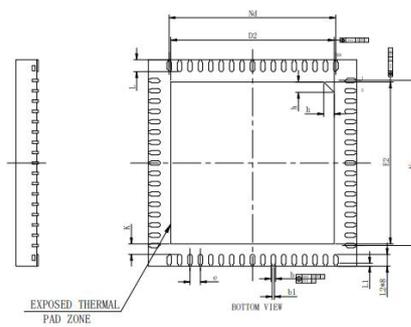
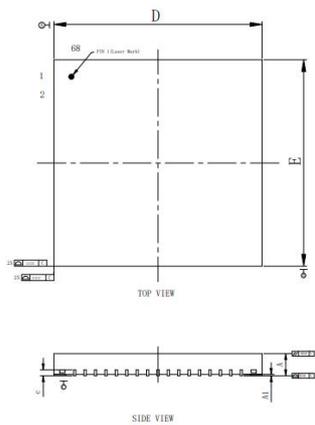
1.5. Package Information

The TXW818 series models are listed in the table below:

Table 1-5-1 Package Information

Model Number	Package	Size	Packaging
TXW818-C0xL	QFN68	7x7	

1.6. Package Dimension Diagram



** 特殊设计: 无

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.39	5.49	5.59
e	0.35BSC		
Nd	5, 60BSC		
E	6.90	7.00	7.10
E2	5.39	5.49	5.59
Ne	5, 60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
L2	0.30	0.40	0.50
K	0.20	—	—
h	0.30	0.35	0.40
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		
fff	0.05		

Figure 1-6-1 QFN68 Package Outline Diagram (POD)

1.7. Pin Description

1.7.1. Analog Pin Specific Functions

Table 1-7-1-1 Pin Specific Analog Function Table

Pin Number TXW818-C0xL	Pin Name	Pin Type	Pin Description
35	VCC	AI	Digital IO power supply, 3.3V. Power supply for PB[0:5], PC6(USBDP), PC7(USBDM), PA[0:15], PC[8:15].
39	VDD	AI/O	Digital system power supply, default internal LDO output 1.1V. For low-power applications, an external DCDC can be used.
42	VCC18	AO	Internal LDO 1.8V output. Power supply for the chip's internal PSRAM.
41	VCCA	AI	Power supply for analog modules, 3.3V.
2	VCCRF	AI	Power supply for RF module, 3.3V.
1	VCCPA	AI	Power supply for RF PA, 3.3V.
37	VCCP	AI	Power supply for BUCK input, 3.3V.
38	BOUT	AO	Buck DCDC output. External inductor pin for the BUCK module. Recommended inductance: 4.7uH, self-resonant frequency > 10MHz, DCR < 400mΩ, saturation current > 500mA.
40	VCCD	AI	Input power supply for internal VDD LDO. Accepts external power supply of 1.8V - 3.3V. When using internal BUCK, VCCD serves as the feedback pin for the BUCK. If the package does not have a separate VCCD pin, it is internally connected to VCCA. Detailed description is in the hardware design guide.
67	VDD15R	AI	RF power supply, 1.8V.
66	VDD15L	AI	RF LO power supply, 1.8V.
65	VDD15O	AO	Internal LDO output power supply, sourced from VCCA, used to supply power to VDD15L and VDD15R, 1.8V.
36	VCAM	AI/O	Internal LDO output or external power supply input; also supplies power to digital IOs PB[6:15] and PC[0:5]. When powered internally, supports 2.5V - 2.8V or 3.3V. When powered externally, supports 1.8V - 3.3V.
62	VCMAU	AO	Internal reference output, no load capability.
60	V33AUDIO	AI	Power supply for audio module, recommended independent power supply of 3.3V (must be turned off

			when the device is in sleep mode), or connected to VCAM (2.8 - 3.3V).
59	AUDIOVDD	AO	Power supply for audio module, supports internal 2.7V output, used as bias power supply for external analog MIC.
58	DACOUT	AO	Audio DAC output.
61	MICP	AI	Microphone input P terminal.
63	XI	AI	High-speed crystal oscillator input.
64	XO	AO	High-speed crystal oscillator output.
68	ANT	AI/O	RF antenna port.
GND	EPAD	AI	Ground.

Notes:

- 1) IO in the VCAM power domain is in high impedance state only when VCAM is powered (VCAM is off by default when the chip is powered on).
- 2) Do not use two GPIOs in the same path simultaneously as analog ADC.
- 3) Comparator P/N terminals must be used in pairs.

Table 1-7-1-2 Pin Specific Analog Function Table

Pin Name	I/O Type	Function Description Default State	Power Domain	ADC Path (Arbitrary Sampling)	Comparator Path (P/N Compare)	Special Function
HSDP	A	USB	VCC			Digital IO: PC6
HSDM	A	USB	VCC			Digital IO: PC7
PA0	I/O	High-impedance Input	VCC	ADKEY_N0	CMP_P0	
PA1	I/O	High-impedance Input	VCC			
PA2	I/O	High-impedance Input	VCC			Low Power PWM0
PA3	I/O	High-impedance Input	VCC			Low Power PWM1
PA4	I/O	High-impedance Input	VCC			
PA5	I/O	High-impedance Input	VCC			
PA6	I/O	High-impedance Input	VCC			
PA7	I/O	High-impedance Input	VCC			
PA15	I/O	High-impedance Input	VCC			
PA8	I/O	High-impedance Input	VCC			ADKEY_N1
PA9	I/O	Input Pull-up 100KΩ	VCC			
PA10	I/O	Input Pull-up 100KΩ	VCC			
PA11	I/O	High-impedance Input	VCC	Low Power PWM3		
PA12	I/O	High-impedance Input	VCC	Low-speed Crystal Oscillator Output		
PA13	I/O	High-impedance Input	VCC	Low-speed Crystal Oscillator Input		
PA14	I/O	High-impedance Input	VCC			

PB6	I/O	High-impedance Input	VCAM	ADKEY_N2	CMP_N2	
PB7	I/O	High-impedance Input	VCAM			
PB8	I/O	High-impedance Input	VCAM			
PB9	I/O	High-impedance Input	VCAM			
PB10	I/O	High-impedance Input	VCAM			
PB11	I/O	High-impedance Input	VCAM			
PB12	I/O	High-impedance Input	VCAM			
PB13	I/O	High-impedance Input	VCAM			
PB14	I/O	High-impedance Input	VCAM			
PB15	I/O	High-impedance Input	VCAM			
PC0	I/O	High-impedance Input	VCAM	ADKEY_P0	CMP_P2	
PC1	I/O	High-impedance Input	VCAM			
PC2	I/O	High-impedance Input	VCAM			
PC3	I/O	High-impedance Input	VCAM			
PC4	I/O	High-impedance Input	VCAM			
PC5	I/O	High-impedance Input	VCAM			
PC8	I/O	High-impedance Input	VCC	ADKEY_P1	CMP_P3	
PC9	I/O	High-impedance Input	VCC			
PC10	I/O	High-impedance Input	VCC			
PC11	I/O	High-impedance Input	VCC			
PC12	I/O	High-impedance Input	VCC			
PC13	I/O	High-impedance Input	VCC			
PC14	I/O	High-impedance Input	VCC			
PC15	I/O	High-impedance Input	VCC			
PE0	I/O	High-impedance Input	VCC		CMP_N0	
PE2	I/O	High-impedance Input	VCC			
PE17	I/O	High-impedance Input	VCC			
PE1	I/O	High-impedance Input	VCC		CMP_P1	
PE3	I/O	High-impedance Input	VCC			

1.7.2. Digital Pin Specific Functions

Table 1-7-2-1 GPIO Pin Specific Digital Function

Pin Name	I/O Type	Function Description Default State	Power Domain	multiplexing function 0	multiplexing function 1	multiplexing function 2	multiplexing function 3
PA0	I/O	High-impedance Input	VCC	lcd_data5	lcd_te	rmii_rxd1	lcd_data15
PA1	I/O	High-impedance Input	VCC	lcd_data6	lcd_te	rmii_ref_clkln	lcd_data16
PA2	I/O	High-impedance Input	VCC	lcd_data7	qspi_io0	ospi_io0	
PA3	I/O	High-impedance Input	VCC	qspi_io1	qspi_io3	ospi_io3	ospi_io1
PA4	I/O	High-impedance Input	VCC	lcd_data8	rmii_rxd2	rmii_txd0	lcd_data17

PA5	I/O	High-impedance Input	VCC	lcd_data9	rmii_rxd3	rmii_txd1	lcd_data18
PA6	I/O	High-impedance Input	VCC	lcd_data10		rmii_tx_en	lcd_data19
PA7	I/O	High-impedance Input	VCC	lcd_data11		ospi_nss0	rmii_crs_dv
PA8	I/O	High-impedance Input	VCC	sd_dat0	qspi_clk	ospi_clk	rmii_rx_er
PA9	I/O	Input Pull-up 100KΩ	VCC	sd_clk	qspi_io2	ospi_io2	
PA10	I/O	Input Pull-up 100KΩ	VCC	sd_cmd	qspi_io1	ospi_io1	
PA11	I/O	High-impedance Input	VCC	lcd_data12	qspi_io2	ospi_io2	
PA12	I/O	High-impedance Input	VCC	lcd_data13	qspi_io1	ospi_io1	lcd_data20
PA13	I/O	High-impedance Input	VCC	lcd_data14	qspi_io0	ospi_io0	lcd_data21
PA14	I/O	High-impedance Input	VCC	lcd_data15	qspi_io3	ospi_io3	lcd_data23
PA15	I/O	High-impedance Input	VCC	lcd_data4	lcd_te	rmii_rxd0	lcd_data14
PB0	I/O	High-impedance Input	VCC		sd_dat1		
PB1	I/O	High-impedance Input	VCC		sd_dat0		
PB2	I/O	High-impedance Input	VCC		sd_clk		
PB3	I/O	High-impedance Input	VCC		sd_cmd		
PB4	I/O	High-impedance Input	VCC		sd_dat3		
PB5	I/O	High-impedance Input	VCC		sd_dat2		lcd_data23
PB6	I/O	High-impedance Input	VCAM	sd_dat1	dvp_vsync	lcd_data0	lcd_data8
PB7	I/O	High-impedance Input	VCAM	sd_dat0	dvp_hsync	lcd_data1	lcd_data9
PB8	I/O	High-impedance Input	VCAM	sd_clk	dvp_data_in7	lcd_data2	lcd_data10
PB9	I/O	High-impedance Input	VCAM	sd_cmd	dvp_mclk	lcd_data3	lcd_data11
PB10	I/O	High-impedance Input	VCAM	sd_dat3	dvp_data_in6	lcd_data4	lcd_data12
PB11	I/O	High-impedance Input	VCAM	sd_dat2	dvp_data_in5	lcd_data5	lcd_data13
PB12	I/O	High-impedance Input	VCAM	rmii_rxd0	dvp_pixel_clk_in	lcd_data6	lcd_data14
PB13	I/O	High-impedance Input	VCAM	rmii_rxd1	dvp_data_in4	lcd_data7	lcd_data15
PB14	I/O	High-impedance Input	VCAM	rmii_ref_clkin	dvp_data_in0	lcd_dotclk_or_rwr	lcd_data16
PB15	I/O	High-impedance Input	VCAM	rmii_txd0	dvp_data_in3	lcd_hsync_or_dc	lcd_data17
PC0	I/O	High-impedance Input	VCAM	rmii_txd1	dvp_data_in1	lcd_vsync_or_cs	lcd_data18
PC1	I/O	High-impedance Input	VCAM	rmii_tx_en	dvp_data_in2	lcd_de_or_erd	lcd_data19
PC2	I/O	High-impedance Input	VCAM	rmii_crs_dv		lcd_data8	lcd_data20
PC3	I/O	High-impedance Input	VCAM	rmii_rx_er		lcd_data9	lcd_data21
PC4	I/O	High-impedance Input	VCAM	rmii_rxd2		lcd_data10	lcd_data22
PC5	I/O	High-impedance Input	VCAM	rmii_rxd3		lcd_data11	lcd_data23
PC6	I/O	High-impedance Input	VCC				
PC7	I/O	High-impedance Input	VCC				
PC8	I/O	High-impedance Input	VCC	lcd_data0	ospi_io3	rmii_rxd0	qspi_io3
PC9	I/O	High-impedance Input	VCC	lcd_data1	ospi_io4	rmii_rxd1	
PC10	I/O	High-impedance Input	VCC	lcd_data2	ospi_clk	rmii_ref_clkin	qspi_clk
PC11	I/O	High-impedance Input	VCC	lcd_data3	ospi_io5	rmii_txd0	rmii_rxd2
PC12	I/O	High-impedance Input	VCC	lcd_data4	ospi_nss0	rmii_txd1	rmii_rxd3
PC13	I/O	High-impedance Input	VCC	lcd_data5	ospi_io6	rmii_tx_en	

PC14	I/O	High-impedance Input	VCC	lcd_data6	ospi_io1	rmii_crs_dv	qspi_io1
PC15	I/O	High-impedance Input	VCC	lcd_data7	ospi_io7	rmii_rx_er	
PE0	I/O	High-impedance Input	VCC	lcd_dotclk_or_rwr	ospi_io2		qspi_io2
PE1	I/O	High-impedance Input	VCC	lcd_hsync_or_dc	ospi_dqs		
PE2	I/O	High-impedance Input	VCC	lcd_vsync_or_cs	ospi_io0		qspi_io0
PE3	I/O	High-impedance Input	VCC	lcd_de_or_erd	ospi_reset0		
PE17	I/O	High-impedance Input	VCC				

1.7.3. Digital Pin Output Arbitrary Mapping Function

Note:

PB[0:5] and PE17 are not mapped to any functions; other digital IOs can be flexibly configured.

Table 1-7-3-1 Arbitrary Mapping Table for GPIO Output Functions

Function Number	Function Name	Function Description
1	COMP_DOUT_DIG0	Comparator 0 Digital IO Output
2	COMP_DOUT_DIG1	Comparator 1 Digital IO Output
3	GRANT_BLE_SWITCH_O	Bluetooth Coexistence Switch Signal
4	GRANT_BLE	Bluetooth Coexistence BLE Arbitration Signal
5	GRANT_WI-FI_SWITCH_O	Bluetooth Coexistence WI-FI SWITCH Signal
6	RF_SWITCH_EN1	External RF Switch Enable 1
7	RF_SWITCH_EN0	External RF Switch Enable 0
8	ANTENNA_SEL	Dual Antenna Selection Signal
9	PA_EN	External PA Enable Signal
10	RF_EXT_LNA_EN	External RF LNA Enable Signal
11	RF_TX_EN_FEM	External RF FEM Transmit Enable
12	RF_RX_EN_FEM	External RF FEM Receive Enable
13	UART4_TX	UART4 TX Output
14	UART5_TX	UART5 TX Output
15	UART0_RTS_RE_O	UART0 RTS RE Output
16	UART0_CTS_DE_OUT	UART0 RTS DE Output
17	UART0_OUT	UART0 TX Output
18	STMR5_PWM_OUT	SIMPLE TIMER5 PWM Output
19	STMR4_PWM_OUT	SIMPLE TIMER4 PWM Output
20	STMR3_PWM_OUT	SIMPLE TIMER3 PWM Output
21	STMR2_PWM_OUT	SIMPLE TIMER2 PWM Output
22	STMR1_PWM_OUT	SIMPLE TIMER1 PWM Output
23	STMR0_PWM_OUT	SIMPLE TIMER0 PWM Output
24	TMR3_PWM_OUT	TIMER3 PWM Output

25	TMR2_PWM_OUT	TIMER2 PWM Output
26	TMR1_PWM_OUT	TIMER1 PWM Output
27	TMR0_PWM_OUT	TIMER0 PWM Output
28	LED_TMR0_PWM_OUT	LED TIMER0 PWM Output
29	LED_TMR1_PWM_OUT	LED TIMER1 PWM Output
30	LED_TMR2_PWM_OUT	LED TIMER2 PWM Output
31	LED_TMR3_PWM_OUT	LED TIMER3 PWM Output
32	SDHOST_SCLK_O	SDC HOST SDCLK Output
33	SDHOST_CMD_OUT	SDHOST CMD Output
34	SDHOST_DAT0_OUT	SDHOST DAT0 Output
35	SDHOST_DAT1_OUT	SDHOST DAT1 Output
36	SDHOST_DAT2_OUT	SDHOST DAT2 Output
37	SDHOST_DAT3_OUT	SDHOST DAT3 Output
38	PDM_MCLK	PDM MCLK Output
39	QSPI_NSS1_OUT	QSPI Chip Select 1 Output
40	SPI0_NSS_OUT	SPI0 Chip Select Output
41	SPI0_SCK_OUT	SPI0 CLK Output
42	SPI0_IO0_OUT	SPI0 IO0 Output
43	SPI0_IO1_OUT	SPI0 IO1 Output
44	SPI0_IO2_OUT	SPI0 IO2 Output
45	SPI0_IO3_OUT	SPI0 IO3 Output
46	SPI1_NSS_OUT	SPI1 Chip Select Output
47	SPI1_SCK_OUT	SPI1 CLK Output
48	SPI1_IO0_OUT	SPI1 IO0 Output
49	SPI1_IO1_OUT	SPI1 IO1 Output
50	SPI1_IO2_OUT	SPI1 IO2 Output
51	SPI1_IO3_OUT	SPI1 IO3 Output
52	SPI2_NSS_OUT	SPI2 Chip Select Output
53	SPI2_SCK_OUT	SPI2 CLK Output
54	SPI2_IO0_OUT	SPI2 IO0 Output
55	SPI2_IO1_OUT	SPI2 IO1 Output
56	SPI2_IO2_OUT	SPI2 IO2 Output
57	SPI2_IO3_OUT	SPI2 IO3 Output
58	IIS0_MCLK_OUT	IIS0 MCLK Output
59	IIS0_WSCLK_OUT	IIS0 WS Output
60	IIS0_BCLK_OUT	IIS0 BCLK Output
61	IIS0_DO	IIS0 DAT Output
62	IIS1_MCLK_OUT	IIS1 MCLK Output
63	IIS1_WSCLK_OUT	IIS1 WS Output
64	IIS1_BCLK_OUT	IIS1 BCLK Output
65	IIS1_DO	IIS1 DAT Output
66	CLK_TO_IO	Clock Source IO Output
67	LCD_DOTCLK_OR_RWR	LCD Display Interface DOTCLK/RWR Output

68	LCD_VSYNC_OR_CS	LCD Display Interface VSYNC/CS Output
69	LCD_HSYNC_OR_DC	LCD Display Interface HSYNC/DC Output
70	LCD_DE_OR_ERD	LCD Display Interface DE/ERD Output
71	LCD_DAT0	LCD Display Interface Data Bit 0 Output
72	LCD_DAT1	LCD Display Interface Data Bit 1 Output
73	LCD_DAT2	LCD Display Interface Data Bit 2 Output
74	LCD_DAT3	LCD Display Interface Data Bit 3 Output
75	LCD_DAT4	LCD Display Interface Data Bit 4 Output
76	LCD_DAT5	LCD Display Interface Data Bit 5 Output
77	LCD_DAT6	LCD Display Interface Data Bit 6 Output
78	LCD_DAT7	LCD Display Interface Data Bit 7 Output
79	LCD_DAT8	LCD Display Interface Data Bit 8 Output
80	LCD_DAT9	LCD Display Interface Data Bit 9 Output
81	LCD_DAT10	LCD Display Interface Data Bit 10 Output
82	LCD_DAT11	LCD Display Interface Data Bit 11 Output
83	LCD_DAT12	LCD Display Interface Data Bit 12 Output
84	LCD_DAT13	LCD Display Interface Data Bit 13 Output
85	LCD_DAT14	LCD Display Interface Data Bit 14 Output
86	LCD_DAT15	LCD Display Interface Data Bit 15 Output
87	LCD_DAT16	LCD Display Interface Data Bit 16 Output
88	LCD_DAT17	LCD Display Interface Data Bit 17 Output
89	LCD_DAT18	LCD Display Interface Data Bit 18 Output
90	LCD_DAT19	LCD Display Interface Data Bit 19 Output
91	LCD_DAT20	LCD Display Interface Data Bit 20 Output
92	LCD_DAT21	LCD Display Interface Data Bit 21 Output
93	LCD_DAT22	LCD Display Interface Data Bit 22 Output
94	LCD_DAT23	LCD Display Interface Data Bit 23 Output

1.7.4. Digital Pin Input Arbitrary Mapping Function

Note:

PB[0:5] and PE17 are not mapped to any functions; other digital IOs can be flexibly configured.

Table 1-7-4-1 Arbitrary Mapping Table for GPIO Input Functions

Function Number	Function Name	Function Description
1	TMR0_CAP_IN	Timer0 Capture Input
2	TMR0_SYNC_IN/ext_rfswitch_en0_in	Timer0 Synchronization Input/External RF Switch Enable 0 Input
3	TMR1_CAP_IN	Timer1 Capture Input
4	TMR2_CAP_IN	Timer2 Capture Input
5	TMR3_CAP_IN	Timer3 Capture Input
6	PDM_DATA_IN	PDM DATA Input

7	PTA_REQ_in	PTA REQ Input
8	PTA_PRI_in	PTA PRI Input
9	FREQ_IND_IN	FREQ IND Input
10	STMR0_CAP_IN/LCD_D3_IN	Simple Timer0 Capture Input/LCD_D3_IN Input
11	STMR1_CAP_IN/LCD_D4_IN	Simple Timer1 Capture Input/LCD_D4_IN Input
12	STMR2_CAP_IN/LCD_D5_IN	Simple Timer2 Capture Input/LCD_D5_IN Input
13	STMR3_CAP_IN/LCD_D6_IN	Simple Timer3 Capture Input/LCD_D6_IN Input
14	PORT_WKUP_IN0	IO Wake-up Channel 0 Input
15	PORT_WKUP_IN1/LCD_D7_IN	IO Wake-up Channel 1 Input/LCD_D7_IN Input
16	PORT_WKUP_IN2/LCD_D8_IN	IO Wake-up Channel 2 Input/LCD_D8_IN Input
17	PORT_WKUP_IN3/LCD_TE	IO Wake-up Channel 3 Input/LCD_TE Input
18	UART0_IN	UART0 RX Input
19	UART0_CTS_DE_IN	UART0 CTS/DE Input
20	UART1_IN/LCD_D9_IN	UART1 RX Input/LCD_D9_IN Input
21	UART1_CTS_DE_IN/LCD_D10_IN	UART1 CTS/DE Input/LCD_D10_IN Input
22	FB_IN/EXT_PA_EN/SYS_NMI	FB_IN/EXT_PA Enable Input/SYS_NMI Input
23	UART4_IN	UART4 RX Input
24	LCD_D0_IN	LCD_D0_IN Input
25	SPI0_NSS_IN	SPI0 NSS Input
26	SPI0_SCK_IN	SPI0 SCK Input
27	SPI0_IO0_IN	SPI0 IO0 Input
28	SPI0_IO1_IN	SPI0 IO1 Input
29	SPI0_IO2_IN	SPI0 IO2 Input
30	SPI0_IO3_IN	SPI0 IO3 Input
31	SPI1_NSS_IN/LCD_D11_IN	SPI1 NSS Input/LCD_D11_IN Input
32	SPI1_SCK_IN	SPI1 SCK Input
33	SPI1_IO0_IN	SPI1 IO0 Input
34	SPI1_IO1_IN/LCD_D12_IN	SPI1 IO1 Input/LCD_D12_IN Input
35	LCD_D1_IN	LCD_D1_IN Input
36	LCD_D2_IN	LCD_D2_IN Input
37	SPI2_NSS_IN/LCD_D13_IN	SPI2 NSS Input/LCD_D13_IN Input
38	SPI2_SCK_IN	SPI2 SCK Input
39	SPI2_IO0_IN	SPI2 IO0 Input
40	SPI2_IO1_IN/LCD_D14_IN	SPI2 IO1 Input/LCD_D14_IN Input
41	SPI2_IO2_IN/LCD_D15_IN	SPI2 IO2 Input/LCD_D15_IN Input
42	SPI2_IO3_IN/LCD_D16_IN	SPI2 IO3 Input/LCD_D16_IN Input
43	STMR4_CAP_IN/LCD_D17_IN	Simple Timer4 Capture Input/LCD_D17_IN Input
44	STMR5_CAP_IN/LCD_D18_IN	Simple Timer5 Capture Input/LCD_D18_IN Input
45	SDHOST_CMD_IN	SDHOST CMD Input
46	SDHOST_DAT0_IN	SDHOST DAT0 Input
47	SDHOST_DAT1_IN	SDHOST DAT1 Input
48	SDHOST_DAT2_IN	SDHOST DAT2 Input

49	SDHOST_DAT3_IN	SDHOST DAT3 Input
50	IIS0_MCLK_IN/LCD_D19_IN	IIS0 MCLK Input/LCD_D19_IN Input
51	IIS0_WSCLK_IN/LCD_D20_IN	IIS0 WS Input/LCD_D20_IN Input
52	IIS0_BCLK_IN/LCD_D21_IN	IIS0 BCLK Input/LCD_D21_IN Input
53	IIS0_DAT_IN	IIS0 DAT Input
54	IIS1_MCLK_IN/UART5_IN/LCD_D22_IN	IIS1 MCLK Input/UART5 RX Input/LCD_D22_IN Input
55	IIS1_WSCLK_IN/LCD_D23_IN	IIS1 WS Input/LCD_D23_IN Input
56	SPI1_IO2_IN/IIS1_BCLK_IN	SPI1 IO2 Input/IIS1 BCLK Input
57	SPI1_IO3_IN/IIS1_DAT_IN	SPI1 IO3 Input/IIS1 DAT Input

2. Function Description

2.1. Processor and Memory

2.1.1. CPU

The TXW818 series chip features the CK803 processor with a maximum clock frequency of 240MHz, characterized by:

- Reduced Instruction Set Computer (RISC) architecture
- 32-bit data, 16-bit/32-bit mixed instruction encoding
- 3-stage pipeline
- 32KB cache
- Single-cycle fast hardware multiplier
- Vector interrupt controller and tick timer
- Interrupt response delay of only 13 processor cycles

2.1.2. Memory

The TXW818 series chip includes:

- ROM: BOOTLOADER and partial kernel functions
- 272KB SRAM: Data and instruction space
- 54Bit EFUSE: For keys and custom usage

2.1.3. Memory Expansion

The TXW818 series chip supports memory expansion, supporting SPI Flash and PSRAM via the SPI interface (some chips have built-in). The on-chip QSPI controller supports external QSPI Flash and PSRAM (up to two memory expansions), and supports XIP functionality. QSPI supports external memory up to 32MB of Flash and PSRAM address space mapping.

2.2. System Clock

The TXW818 series chip clock sources include:

- 128KHz LIRC
- 10MHz HIRC
- 32.768KHz low-speed crystal oscillator
- 24~50MHz high-speed crystal oscillator
- 480MHz fractional USB2.0 PLL
- External IO input clock source

2.3. Analog Peripherals

2.3.1. Analog-to-Digital Converter (SARADC)

The TXW818 series chip integrates one 12-bit comparator and one 12-bit SARADC, which can operate in ADC/DAC mode, with the following features:

- Supports up to 1MHz clock input
- Up to 62.5Ksps
- Supports 12-bit ADC/DAC conversion accuracy
- Supports basic timers 0/1/2/3, simple timers 0/1/2/3/4/5, and software-triggered ADC conversions

2.3.2. Temperature Sensor

The TXW818 series chip integrates a temperature sensor that samples the voltage of the temperature sensor via an internal ADC channel to calculate the internal temperature of the chip.

2.3.3. USB2.0

The TXW818 series chip integrates USB2.0 Controller and USB2.0 PHY, compatible with standard USB2.0 High/Full Speed Host & Device protocols.

The TXW818 series chip features high-performance USB2.0 high-speed PHY with a self-developed innovative CDR patent technology that ensures reliable operation even in harsh environments, supporting high-speed mode with a theoretical speed of up to 480Mbps without an external USB2.0 PHY. Supports crystal-less USB. When USB2.0 functionality is not needed, it can be used as two GPIOs.

2.3.4. XOSC

The TXW818 series chip integrates a high-speed crystal oscillator circuit module that requires an external 24~50MHz passive crystal oscillator.

2.3.5. PLL

The TXW818 series chip integrates a high-performance 480MHz fractional USB2.0 PLL.

2.3.6. Audio ADC

The TXW818 series chip includes one delta-sigma audio ADC with an integrated PGA, supporting single-ended and differential analog microphone inputs:

- AUDIO Codec supports 8/11.025/12/16/22.05/24/32/44.1/48 KHz sampling rates
- Supports high-performance single-ended and differential input analog mics with integrated PGA
- Supports howl suppression
- Supports G711 A-law codec
- Supports VAD (voice action detect) event generation

2.3.7. Audio DAC

The TXW818 series chip includes one delta-sigma audio DAC.

2.4. Digital Peripherals

2.4.1. GPIO

The TXW818 series chip integrates up to 47 general-purpose GPIOs with the following features:

- Configurable pull-up resistors with values of 4.7K Ω and 100K Ω
- 100K Ω pull-down resistor
- Four levels of IO output drive configurable, ranging from 4/12/20/28mA, each level at 8mA
- Support for open-drain high output
- IO state latch function in low-power mode
- Support for ADC analog input function
- Independent digital IO input and output direction enable, disabling digital IO input/output function

2.4.2. SPI/IIC

The TXW818 series chip integrates three SPI interfaces. SPI0/1/2 all support SPI master/slave mode, and SPI1/2 support either SPI or IIC functionality (one selectable).

The features of the SPI are as follows:

- Support for master and slave modes
- Support for Motorola SPI
- Support for master/slave half-duplex transmission
- Programmable serial clock polarity and phase

-
- Support for four modes:
 - Standard mode: SCLK, CS, IO0 (MOSI), IO1 (MISO), one SCLK transmits 1 bit
 - 3-wire mode: SCLK, CS, IO0, one SCLK transmits 1 bit
 - DUAL mode: SCLK, CS, IO0, IO1, one SCLK transmits 2 bits
 - QUAL mode: SCLK, CS, IO0, IO1, IO2, IO3, one SCLK transmits 4 bits
 - Transfer end flag with MCU interrupt
 - Support for master mode baud rate up to 1/2 of the system clock
 - Support for data width selection from 1 to 32 bits
 - Support for DMA (direct memory access)
 - Support for high-byte first or low-byte first

The features of the IIC module are as follows:

- Support for master and slave modes
- Support for master clock synchronization and arbitration
- Support for slave pulling SCL low when data is not ready to send or receive buffer is full
- Support for 7-bit or 10-bit slave address
- Support for DMA

2.4.3. UART

The TXW818 series chip integrates three UART interfaces, with two simple UARTs (UART4/5) and one advanced UART0.

The features of UART0 are as follows:

- Support for 8-bit and 9-bit data modes
- Support for parity check
- Receive buffer for 4 frames of data, transmit buffer for 1 frame of data
- Support for receive and transmit DMA
- Support for hardware flow control, RTS_N and CTS_N have enable signals, configurable to make RTS_N active when receiving buffer has N (N=0, 1, 2, 3) data
- Hardware detection for receive timeout, timeout configuration range: 1~65536 bit rate time
- Support for RS485 mode

The features of UART4/5 are as follows:

- Support for half-duplex
- Support for transmitting 9-bit data
- Support for software parity check

2.4.4. IIS_PCM

The TXW818 series chip integrates two IIS_PCM modules for extended audio functionality with the following features:

- Supports IIS/Left-aligned/Right-aligned/PCM format transmission
- Supports Left Channel/Right Channel/Stereo mode
- Supports Master/Slave mode
- Supports 2-32 bit operational bit width
- Supports output MCLK mode, and also using input MCLK as master/slave clock
- Supports channel swapping
- Supports dual address auto-switching

2.4.5. PDM

The TXW818 series chip integrates one PDM module for extended audio functionality. The PDM module processes the audio interface for digital MEMS microphones and provides a high-precision output clock, supporting left/right channels and stereo mode. The features are as follows:

- Converts PDM data from digital MEMS microphone input to 16-bit PCM data
- Supports Left Channel/Right Channel/Stereo mode
- Provides 50/100 decimation ratio for PDM/PCM modes
- Supports channel swapping
- Supports DMA dual address auto-switching

2.4.6. Camera DVP Interface

The TXW818 series chip integrates one CMOS Sensor DVP interface module for external camera connections with the following features:

- Supports 8-bit parallel interface for Sensor
- Supports HSYNC and VSYNC polarity selection
- Supports HSYNC and VSYNC invalidity detection
- Supports data formats: YUV422 and RAW DATA

2.4.7. VPP Image Processing Module

- Supports YUV data order adjustment
- Supports retaining only Y data
- Supports YUV data range limitation
- Supports YUV image downscaling by 1/2 or 1/3
- Supports Scatter DMA, YUV format only
- Supports time watermark, color frame, motion detection

2.4.8. PRC Data Processing Module

- Supports YUV422 data rearrangement
- Hardware acceleration for optical flow algorithm
- Supports Scatter DMA

2.4.9. Motion JPEG Video Codec

The TXW818 series chip integrates one MJPEG video encoder and one MJPEG video decoder for image/video compression and decompression with the following features:

- Maximum resolution support:
 - 8000*8000 at 2fps (photo mode)
 - 4000*4000 at 5fps (photo mode)
 - 1920*1080 at 30fps
 - 1280*720 at 60fps
 - 640*480 at 120fps
- Supports JPEG0/1 encoding, YUV420 pixel data format
- Supports JPEG1 decoding, YUV420/422 pixel data format
- Supports compressed data dual buffer
- Supports DQT dynamic adjustment
- Supports JPEG header encoding/decoding
- Supports Gather DMA

2.4.10. LCD

The TXW818 series chip integrates one LCD display interface controller and video post-processing hardware module with the following features:

- Supports RGB and MCU (8080 & 6800) interfaces
- Supports image scaling, 90/180/270 degree rotation, horizontal and vertical mirroring
- Supports image OSD, Alpha Blending
- Supports CCM, Gamma correction, saturation, and contrast adjustment
- Supports 2D-GDMA
- RGB push screen supports up to 1280*720 @ 50fps

2.4.11. Video Stream Path

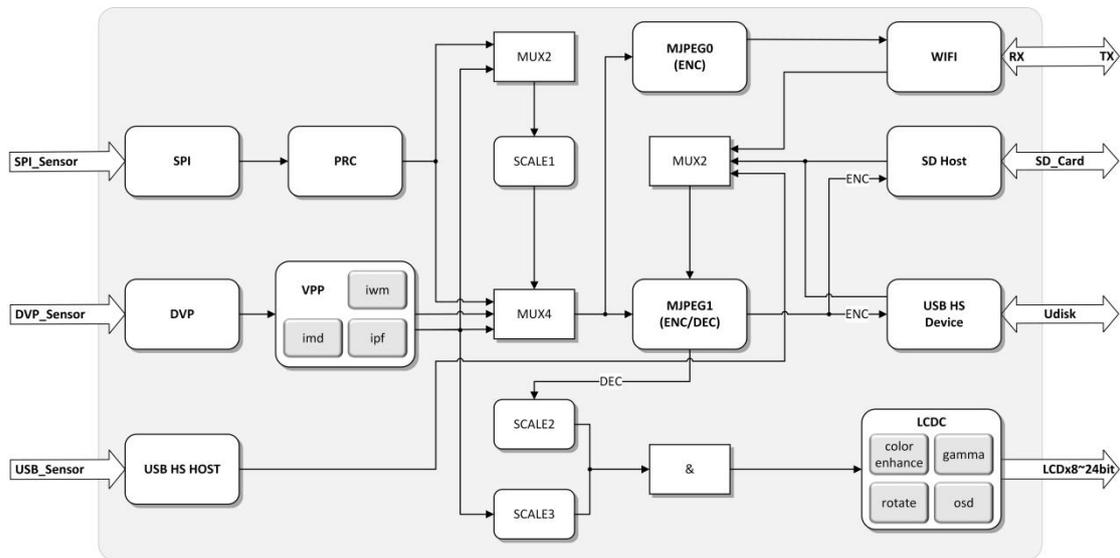


Figure 2-4-9-1 Video Codec and Display Subsystem Data Flow Architecture Diagram

2.4.12. Ethernet Controller MAC

The TXW818 series chip integrates one MAC module for wired Ethernet connection with the following features:

- Supports 10/100Mbps
- Supports RMII interface
- Supports half-duplex and full-duplex modes
- Supports up to 16 MAC address filtering
- Supports "ring" descriptor structure
- Complies with IEEE 802.3 CSMA/CD standard

2.4.13. SDIO2.0 Device Controller

The TXW818 series chip integrates one SDIO2.0 Device controller module, supporting SD 1/4bit mode and SDIO SPI mode with a maximum clock speed of 50MHz. It is used for SDIO host interfaces to conveniently connect and extend Wi-Fi applications.

2.4.14. SD HOST Controller

The TXW818 series chip integrates one SD host controller module, supporting SD 1/4bit mode with a maximum clock speed of 50MHz. It is used to extend external SD storage cards or SDIO device interface devices.

2.4.15. M2M DMA Module

The TXW818 series chip integrates two memory-to-memory DMA controller modules for DMA data transfer within the chip's SRAM. Features include:

- Supports byte alignment
- Supports up to 64KB per transfer
- Supports memcpy and memset modes
- Supports 4-word buffer
- Supports transfer completion flags and interrupts

2.5. Timer Resources

2.5.1. Basic Timers

The TXW818 series chip integrates four Normal timers. Timer0/3 are 32-bit timers, and Timer1/2 are 16-bit timers with DMA and infrared functions.

The following description pertains specifically to the 16-bit counter timer1, while timer0/3 are defined as 32-bit timers.

Timer1 consists of a 16-bit auto-reload counter capable of measuring the pulse width of input signals (input capture) or generating output waveforms (output compare, PWM, etc.). Main features include:

- 16-bit incrementing counter
- Programmable prescaler (can be modified in real time), supporting up to 128x division
- Supports GPIO as clock source
- Supports different clock sources
- Allows updating timer period register after each cycle
- Supports input capture function:
 - Supports saving up to one capture event pointer at a time
 - Each capture event's polarity can be independently configured
 - Configurable to reset the counter value on each capture event occurrence
- PWM output
- Supports auto-reload for period and duty cycle
- External signal control for synchronization
- Supports infrared function

2.5.2. Simple Timers

The TXW818 series chip integrates one simple timer with six 32-bit basic function timers (stimer0 to stimer5), supporting various clock sources and modes including timer, counter,

capture, and PWM modes.

2.5.3. Watchdog Timer

The TXW818 series chips integrate an independent watchdog module to reset the system in case of anomalies. The watchdog module operating clock is a normally-open 64KHz low-speed RC's 2-division clock, i.e., a clock that operates at 32KHz independent of the system clock. By default, it resets the system every 2 seconds. To avoid this, the watchdog needs to be reset periodically within user programs. The reset interval can be configured between 8ms and 256s, and it can be set to either generate an interrupt or directly reset the system.

2.6. Security Hardware Accelerators

2.6.1. CRC Module

The TXW818 series chips integrate a CRC function module for data verification. Features include:

- Supports polynomial lengths of 5, 7, 8, 16, 32 bits
- Custom polynomial support
- Multiple segmented data CRC verification

2.6.2. AES Module

The TXW818 series chips integrate a system AES function module for data encryption and decryption. Features include:

- AES-128/192/256 ECB/CBC/CTR encryption/decryption
- DMA mode support, with a maximum data length of 1MBytes

2.6.3. SHA Module

The TXW818 series chips integrate a SHA function module for data verification. Features include:

- Supports SHA2-256
- DMA mode support, with a maximum data length of 65536 bytes
- Multiple segmented data SHA operations
- Maximum data rate: 700Mbps @ 240MHz(system clock)

2.6.4. TRNG Module

The TXW818 series chips are integrate a true random number generator module, user data security random seed generation.

3. Electrical Parameters

3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum Value	Maximum Value	Unit
V_{VCC}	Operating Voltage	-	-0.3	3.6	V
V_{VCCA}	Operating Voltage (Analog Section)	-	-0.3	3.6	V
$VCCPA$ $VCCRF$	Operating Voltage (RF Section)	-	-0.3	3.6	V
T_{ST}	Storage Temperature	-	-40	150	°C

Operating outside these limits may cause permanent chip damage. Using the chip within these ratings but outside recommended conditions may affect reliability, function, and performance, and shorten chip lifespan.

3.2. Recommended Operating Conditions

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
V_{VCC}	Operating Voltage	-	3	3.3	3.6	V
V_{VCCA}	Operating Voltage (Analog Section)	-	3	3.3	3.6	V
$VCCPA$ $VCCRF$	Operating Voltage (RF Section)	-	3	3.3	3.6	V
$VCAM^{(1)}$	Vcam LDO Load Capacity	$VCAM = 2.8V$		150		mW
$VCC18$	VCC18 LDO Load Capacity	$VCC18 = 1.8V$		180		mW
T_A	Operating Temperature	-	-40	-	85	°C

(1) Vcam/VCC18 LDO load capacity is specified at 85°C. It increases as temperature

decreases, decreases as VCC voltage decreases, and increases as VCAM voltage level decreases.

Note:

1. With built-in PSRAM packaging, PSRAM itself consumes about 20mA of VCC18 LDO load capacity.

3.3. DC Electrical Characteristics

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
CIN	Pin Capacitance	-	2	-	pF
VIH	High-Level Input Voltage	0.7*VCC	-	VCC+0.3	V
VIL	Low-Level Input Voltage	-0.3	-	0.3*VCC	V
IIH	High-Level Input Current	-	-	50	nA
IIL	Low-Level Input Current	-	-	50	nA
VOH	High-Level Output Voltage	0.9*VCC	-	-	V
VOL2	Low-Level Output Voltage	-	-	0.1*VCC	V
IOH	High-Level Source Current (VCC = 3.3 V, VOH >= 2.64 V, PAD_DRIVER = 3)	-	28	-	mA
IOL	Low-Level Sink Current (VDD1 = 3.3 V, VOL = 0.5 V, PAD_DRIVER = 3)	-	50	-	mA
RPU	Pull-Up Resistor	4.7	100	100	kΩ
RPD	Pull-Down Resistor		100		kΩ
VIH_nRST	Chip MCLR Reset Release Voltage	0.7*VCC	-	VCC+0.3	V
VIL_nRST	Chip MCLR Reset Voltage	-0.3	-	0.3*VCC	V

Note:

1. VOH and VOL are measured under high-impedance load conditions.

3.4. AC Electrical Characteristics

3.4.1. External Clock Source Characteristics

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
f_{xoscM}	User External Clock Frequency			40		MHz
V_{BIAS}	XOSCI/XOSCO Bias Level	-	-	550	-	mV
V_{xoh}	XOSCI Input Pin High-Level Voltage	-	-	0.77	-	V
V_{xol}	XOSCO Input Pin Low-Level Voltage	-	-	0.33	-	V
$Duty_{(xoscM)}$	Duty Cycle	-	42	-	58	%
ACC_{xoscM}	HSE Accuracy	-	-	-	-	ppm
$t_{SU(xoscM)}$	Start-up Time	-	-	5		ms
$I_{VCCA(XOSC)}$	XOSCM Oscillator Power Consumption	Average Power	-	0.7	-	mA

3.4.2. Internal Clock Source Characteristics

Table 3-4-2-1 RC10M Oscillator Characteristics

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
V_{VCCA}	Supply Voltage	-	3	3.3	3.6	V
RC10M	Frequency	Tested after 25°C trim	9	10	11	MHz
ACC_{RC10M}	RC10M Oscillator Accuracy	-40°C ~ 85°C	-6	-	+6	%
$t_{SU(RC10M)}$	RC10M Oscillator Startup Time	-	-	60	-	us
$I_{VCCA(RC10M)}$	RC10M Oscillator Power Consumption	Average Power Consumption	-	-	1	mA

Table 3-4-2-2 RC128K Oscillator Characteristics

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
RC128K	Frequency	TA=25°C	-	128	-	kHz

$I_{DD(RC128K)}$	RC128K Oscillator Power Consumption	-	-	-	-	uA
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3.5. Power Consumption Characteristics

3.5.1. RF Power Consumption

The following power consumption data is based on a 3.3V power supply, 25°C ambient temperature, and CPU running at 120MHz. All transmission data is measured with 100% duty cycle.

RF Power Consumption (100% duty cycle measured)			
Operating Mode	Description		Average(mA)
Active (LDO Mode)	TX	802.11g, 20 MHz, 54 Mbps, 15dBm	240
		802.11n, 20 MHz, MCS7, 15dBm	240
		802.11n, 20 MHz, MCS7, 6dBm	168
	RX	802.11b/g/n, 20 MHz	76

The following power consumption data are estimated:

RF Power Consumption (50% duty cycle measured)			
Operating Mode	Description		Average(mA)
Active (LDO Mode)	TX+RX	802.11g, 20 MHz, 54 Mbps, 15dBm	158
		802.11n, 20 MHz, MCS7, 15dBm	158
		802.11n, 20 MHz, MCS7, 6dBm	122

RF Power Consumption (100% duty cycle measured)			
Operating Mode	Description		Average(mA)
Active (DCDC Mode)	TX	802.11g, 20 MHz, 54 Mbps, 15dBm	216
		802.11n, 20 MHz, MCS7, 15dBm	216
		802.11n, 20 MHz, MCS7, 6dBm	152
	RX	802.11b/g/n, 20 MHz	43

The following power consumption data are estimated:

RF Power Consumption (50% duty cycle measured)			
Operating Mode	Description		Average(mA)
Active (DCDC Mode)	TX+RX	802.11g, 20 MHz, 54 Mbps, 15dBm	129
		802.11n, 20 MHz, MCS7, 15dBm	129
		802.11n, 20 MHz, MCS7, 6dBm	97

3.5.2. CPU Power Consumption

MCU State	WLAN State	TX/RX	Test Conditions	Power Consumption
<i>LP</i> ⁽¹⁾	OFF	-	Constant power domain logic running, 272KB SRAM always on	233.5uA
	OFF	-	Constant power domain logic running, 16KB SRAM always on	31.3uA
<i>ULP</i> ⁽¹⁾	OFF	-	-	28.1uA
Chip powered off	-	-	CHIP_EN = 0	0.7uA

(1) Only supports IO and internal RC wake-up

3.5.3. System Sleep Power Consumption

Description:

The following power consumption data is based on built-in Buck DCDC Mode, 3.6V power supply, 25°C ambient temperature, STA RX Beacon window of 1ms, tested in a shielded environment.

Test Conditions	DTIM1 (uA)	DTIM3 (uA)	DTIM5 (uA)	DTIM6 (uA)	DTIM10 (uA)	DTIM30 (uA)
External 32K	2273	792	490	413	251	178
Internal 32K	2277	804	509	435	288	216

Note:

- 1) When using the internal 32K crystal oscillator, longer sleep times lead to greater errors, thus increasing power consumption.
- 2) Wi-Fi PS Mode power consumption increases in interference environments, and power consumption data may vary under different interference conditions.
- 3) Chips with an "L" designation include built-in and support Buck DCDC, such as TXW818-C04L.

3.6. Reliability

3.6.1.ESD Electrical Characteristics

Symbol	Parameter	Test Conditions	Maximum Value	Unit	Level
ESD	Electrostatic Discharge (Human Body Model, HBM)	TA = + 25°C, JEDEC EIA/JESD22-A114	2000	V	-
	Electrostatic Discharge (Charged Device Model, CDM)	TA = + 25°C, JEDEC EIA/JESD22-C101-B	1000	V	-

3.6.2. Latch-Up Electrical Characteristics

Symbol	Parameter	Test Conditions	Test Type	Minimum Value	Unit
LU	Static latch-up class	JEDEC STANDARD NO.78D	Class I (TA = +25 °C)	±200	mA

3.7.Wi-Fi RF Performance and Power Consumption

3.7.1. Wi-Fi Transmitter Performance

Parameter	Condition	Typical Value(dBm)
Output Power	802.11g, 20 MHz, 54 Mbps	16
	802.11n, 20 MHz, MCS7	16

3.7.2. Wi-Fi Receiver Performance

Parameter	Condition	Typical Value(dBm)
Receiver Sensitivity	HT20 MCS7 4k	-72.5
	NONHT 54M	-74.5
	NONHT 6M	-89.5
	CCK11M	-85

	CCK5.5M	-88
	DSSS2M	-91.5
	DSSS1M	-96

3.7.3. BLE Transmitter Performance

Parameter	Conditions	Typical Value (dBm)
Output Power		20

3.7.4. BLE Receiver Performance

Parameter	Conditions	Typical Value (dBm)
Receive Sensitivity	1Mbps	-94.5

3.8. Audio Performance

3.8.1. Audio ADC Performance

Parameter	Conditions	Typical Value (dBm)
SNR	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	81
THD+N	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	-78

3.8.2. Audio DAC Performance

Parameter	Conditions	Typical Value (dBm)
SNR	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	82
THD+N	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	-75

4. Reference Design

5. Ordering Information

TXW818

C04L

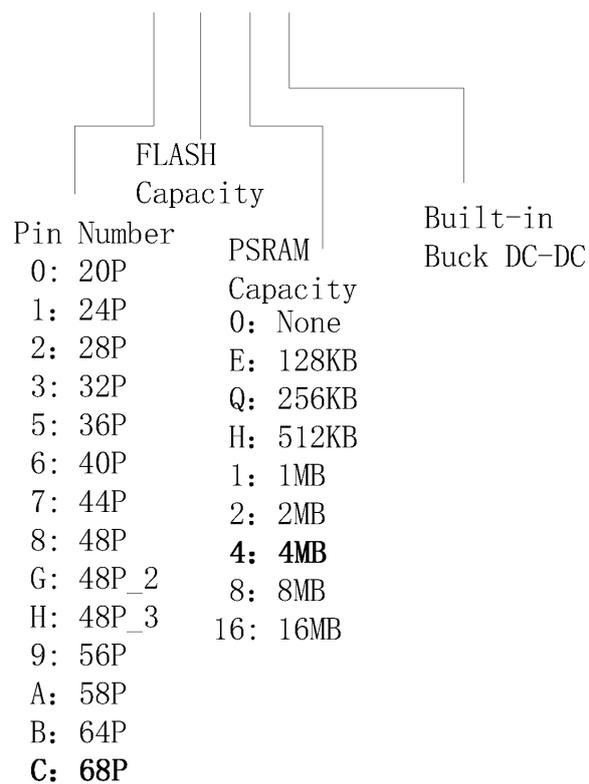


Figure 5-1 Model Naming

Table 5-1 Ordering Information

Product Number	Package	Size	Description
TXW818-C04L	QFN68	7x7	Built-in 32Mbit PSRAM, Buck DC-DC, Video+Audio+Screen Display+Low Power Applications
TXW818-C08L	QFN68	7x7	Built-in 64Mbit PSRAM, Buck DC-DC, Video+Audio+Screen Display+Low Power Applications