泰芯半导体
TaiXin Semiconductor

TXW828-E016FL Datasheet

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Revision History

Date	Version	Description	Revised By
2026-08-06	V1.8	Corrected the VCAM2 LDO load parameters.	TX
2026-07-31	V1.7	Corrected several typographical errors; optimized the descriptions of LDO load and RC8M/RC128K power consumption;	TX
2026-06-15	V1.6	Delete "reference design"; use the hardware reference design as the reference.	TX
2026-06-01	V1.5	Updated MIPI pin description	TX
2026-05-21	V1.4	Added programming port and debug port description (refer to Table 1-7-1-2) Added Wi-Fi sleep keep-alive power consumption data	TX
2026-04-20	V1.3	Corrected analog pin function table	TX
2025-11-20	V1.2	Added "Wake-up I/O Group" column to the analog pin function table; added note item (3)	TX
2025-08-13	V1.1	Optimized VDD power supply description and supplemented RF performance description	TX
2025-07-16	V1.0	Initial release. Specifications are subject to change without notice. Please contact our sales representatives for the latest version.	TX

Contents

1. Product Overview

1.1. Description

The TXW828-E016FL is a low-power, high-performance, highly integrated wireless Audio & Video SoC. It integrates 2.4 GHz Wi-Fi, BLE, and SLE, a high-performance ISP image processor, and an H.264/MJPEG codec, delivering excellent RF performance, superior image processing capability, high encoding quality, and a low bitrate. It also integrates a security algorithm acceleration engine and supports a comprehensive set of peripheral interfaces, including Audio ADC/DAC, MIPI CSI, MIPI DSI, DVP, LCD, RMII MAC, USB 2.0 High-Speed Host/Device, SDMMC Host, I2S, and PDM.

The TXW828-E016FL supports executing programs directly from SPI Flash. It supports RTOS and third-party components, and is accompanied by an open, easy-to-use development and debugging environment.

The TXW828-E016FL is offered in a QFN80 package and supports built-in PSRAM.

Applications:

- Multi-lens IPC/Camera/Video Recorder
- Doorbell, Door Lock
- Other wireless audio/video applications with display output

1.2. Features

- **Wi-Fi MAC & PHY**
  - Compliant with IEEE 802.11 b/g/n standards
  - Supports 1T1R mode at 5/10/20/40 MHz bandwidth; data rate up to 150 Mbps
  - Integrated PA, LNA, and RF switch
  - Supports STA, AP, AP+STA (repeater), and STA+STA operating modes
  - Supports RX STBC (Space Time Block Coding)
  - Supports WPA/WPA2/WPA3
- **BLE**
  - Supports Bluetooth-based fast network provisioning
  - Supports Wi-Fi/BLE PTA coexistence
- **Video Codec**
  - Supports H.264 encoding performance (shared between single- and dual-lens configurations):
  - 1920×1080 @ 30fps + 640×360 @ 30fps + 320×180 @ 30fps
  - Supports H.264 decoding at up to 1920x1080 @ 30fps
  - Supports MJPEG codec with a maximum resolution of 8000×8000; supports 1920×1080 @ 30 fps
  - Supports timestamp watermark, color border frame, motion detection, and hardware-accelerated optical flow algorithm
- **ISP**
  - Maximum supported resolution: 1920×1080 @ 30 fps
  - Supports dual-channel time-division multiplexing
  - Supports 3A (Auto White Balance, Auto Exposure, Auto Focus) and adaptive 2D/3D noise reduction

- Supports Defective Pixel Correction and lens shading correction
- Supports image enhancement including brightness, sharpness, contrast, hue, and saturation adjustment
- Supports motion detection
- Supports infrared (IR) colorization

- **Video Input**
  - Supports DVP, UVC, and SPI camera inputs
  - Supports one 2-lane or two 1-lane MIPI CSI camera
  - Supports H.264/MJPEG decoding, scaling, and re-input
  - Supports BT.656, BT.1120, and BT.601 input
- **Video Output**
  - Supports LCD display via MIPI, RGB, MCU8080, MCU6800, and SPI/QSPI interfaces
  - Supports 1-lane and 2-lane MIPI-DSI
  - Supports display resolution of 1280×720 @ 60 fps
- **Graphic**
  - Supports image scaling, 90°/180°/270° rotation, and horizontal/vertical mirroring
  - Supports two video layers and one OSD layer; the OSD layer supports Alpha Blending
  - Supports denoising, color correction matrix (CCM), gamma correction, saturation adjustment, and contrast adjustment
  - Supports color format conversion
  - Supports 2D DMA
- **Audio**
  - Supports differential-input high-performance analog MIC and built-in PGA
  - Supports one delta-sigma audio ADC channel

- Supports one delta-sigma audio DAC channel
- Supports sample rates of 8/11.025/12/16/22.05/24/32/44.1/48/96 kHz
- Supports PDM and I2S

- **Security**
  - Supports AES 128/192/256 (ECB/CBC/CTR) encryption/decryption
  - Supports SHA1 and SHA2-256
  - Supports 5/7/8/16/32-bit CRC verification
  - Supports SPI Flash firmware encryption protection
  - Supports TRNG (True Random Number Generator)
- **Core**
  - CPU0: XuanTie E804FD with DSP instruction set and hardware floating-point unit (FPU), up to 240 MHz
  - CPU1: XuanTie E804D with DSP instruction set, up to 240 MHz
  - 32KB I-cache, 32KB D-cache
  - 368 KB SRAM (expandable up to 560 KB by powering down select modules)
  - Supports 24–50 MHz external crystal oscillator; 40 MHz recommended
  - Supports RTC (Real-Time Clock)
  - Supports 32 kHz crystal oscillator
  - 19 timers, as follows:
    - 1× always-on 32-bit timer
    - 1× always-on 31-bit timer (supports power-off)
    - 4× 16-bit low-power mode timers with hardware low-power breathing LED support
    - 8× 32-bit timers
    - 2× 16-bit timers supporting IR transceiver and LED strip driving

- 1× 24-bit SysTick timer
- 1× RTCC timer
- 1× read-only 64-bit timer

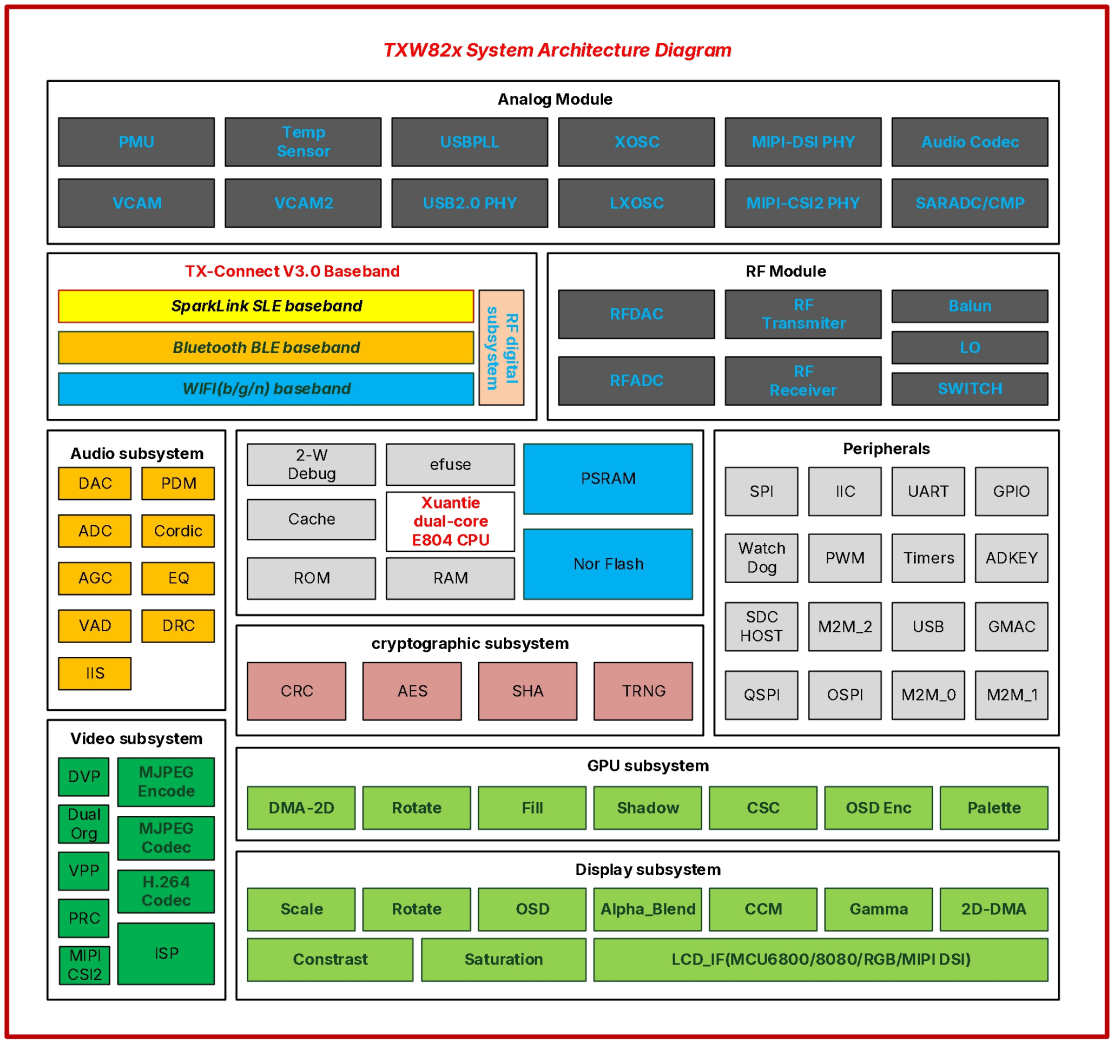
- Supports ULP and LP low-power modes; ULP mode current < 10 μA @ 25°C; supports multi-channel I/O wake-up
- Integrated temperature sensor
- Integrated LVD
- Integrated watchdog for CPU0, CPU1, and the always-on power domain
- Integrated multi-channel LDO outputs with an output voltage range of 1 V to 3.3 V
- 48-bit chip unique identifier (UID)

- **Peripherals**
  - 57 programmable GPIOs with edge- or level-triggered interrupt support
  - 1× 11-bit ADC
  - 2× analog comparators
  - 1× QSPI interface with DTR mode support; supports up to 256 MB external 1.8 V/3.3 V SPI Flash
  - 1× OSPI interface supporting built-in PSRAM
  - 1× 8/10-bit CMOS sensor DVP interface, up to 120 MHz
  - 1× Motion JPEG encoder
  - 1× Motion JPEG codec (encoder/decoder)
  - 1× LCD
  - 2× I2S/PCM interfaces
  - 1× PDM interface
  - 2× SD 2.0 Host Controllers
  - 1× USB 1.1 Full-Speed Device/Host

- 1× USB 2.0 High-Speed Device/Host
- 3× SPI interfaces (Master/Slave); 2 of which are configurable as I2C Master/Slave
- 5× UART interfaces; 2 with hardware flow control and RS-485 support
- 2× IR transmitters (one with IrDA protocol support) and multiple receiver
- 14× PWM outputs (timer-multiplexed); includes 4 independent 16-bit PWM channels with low-power mode support

- **Boot Interface**
  - USB 2.0 Device, UART
  - SPI Flash, SPI NAND Flash, SD NAND, SD/MMC/eMMC
- **Package**
  - QFN80 8x8 package
- **Operating Temperature**
  - -40°C to +85°C

1.3. Functional Block Diagram



Note: NOR Flash is external; PSRAM is built-in.

1.4. Pin Assignment

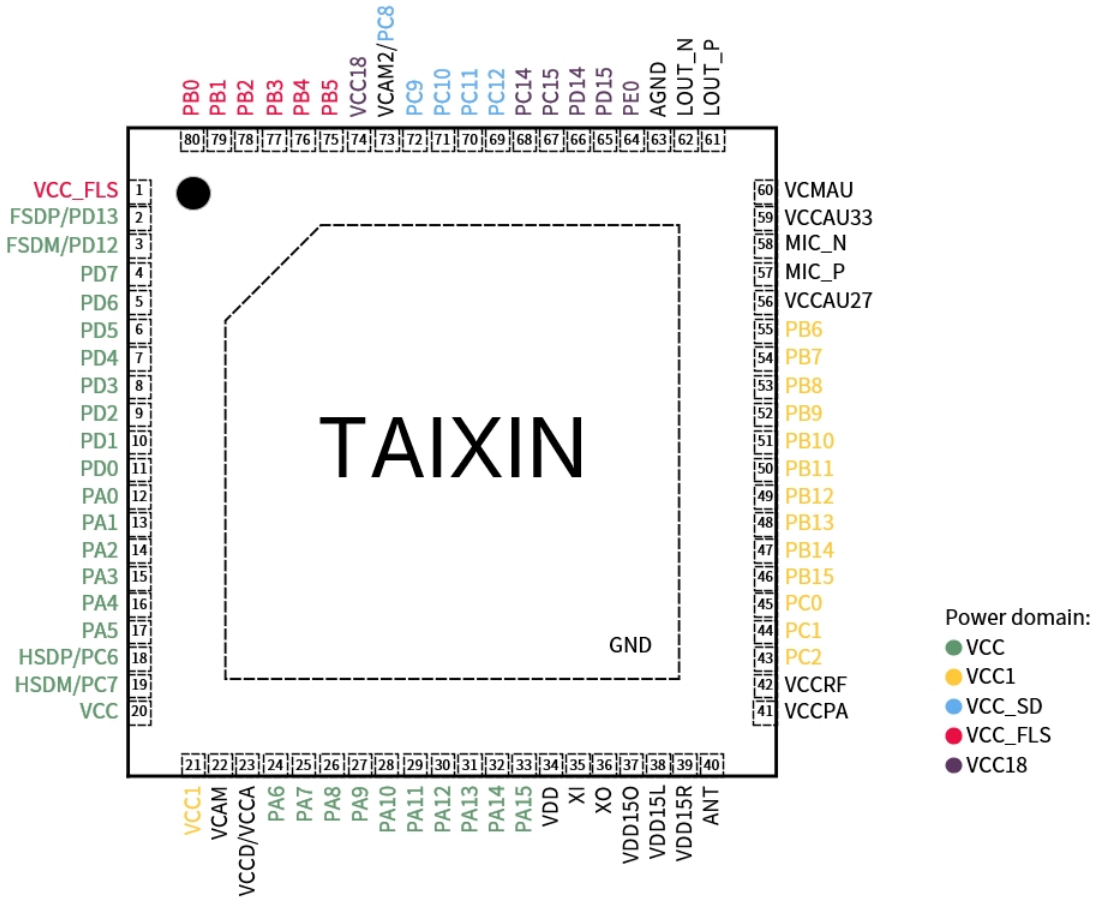


Figure 1-4-1: TXW828-E016FL QFN80 Package Pin Layout

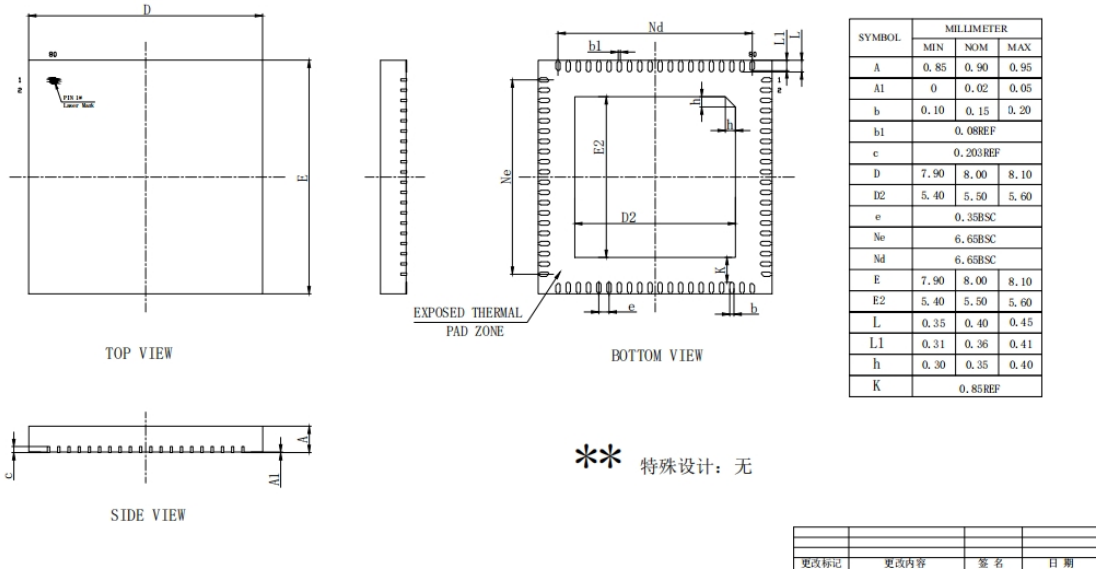
1.5. Package Information

The TXW828-E016FL part number information is listed in the following table:

Table 1-5-1: Package Information

Part Number	Package	Size	Packing
TXW828-E016FL	QFN80	8x8	

1.6. Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.203REF		
D	7.90	8.00	8.10
D2	5.40	5.50	5.60
e	0.35BSC		
Ne	6.65BSC		
Nd	6.65BSC		
E	7.90	8.00	8.10
E2	5.40	5.50	5.60
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
h	0.30	0.35	0.40
K	0.85REF		

更改标记	更改内容	签 名	日 期

Figure 1-6-1: QFN80 Package Outline Drawing (POD)

1.7. Pin Description

1.7.1. Analog Pin Functions

Table 1-7-1-1: Analog Pin Function Table

Pin No. TXW828-E016FL	Pin Name	Pin Type	Pin Description
20	VCC	AI	Digital I/O power supply input, 3.3 V; supplies PA[0:15], PC6 (USBDP), PC7 (USBDM), PD[0:7], and PD[12:13]
21	VCC1	AI	Digital I/O power supply input, 3.3 V; supplies PB[6:15] and PC[0:2]
	VCC_SD (Internal power domain)	AI	Digital I/O power supply; internally selectable between VCC or VCC18 output, 3.3 V/1.8 V; default 3.3 V; supplies PC[8:12]
1	VCC_FLS	AI/O	Digital I/O power supply; internally selectable between VCC or VCC18 output, 3.3 V/1.8 V; default OFF; supplies PB[0:5]
73	VCAM2	AI/O	Internal LDO1 output; supports 1.0 V–2.55 V
34	VDD	AI/O	Digital system power supply; external DCDC 1.15 V supply recommended @ 192 MHz CPU
74	VCC18	AI/O	Internal LDO output; 1.8 V, disabled by default; internal PSRAM power supply; supports 1.0 V–2.55 V; supplies PC[14:15], PD[14:15], and PE0
23	VCCA	AI	Analog module power supply, 3.3 V
42	VCCRF	AI	RF module power supply, 3.3 V
41	VCCPA	AI	RF PA power supply, 3.3 V
23	VCCD	AI	Input power supply for the internal VDD LDO; accepts external supply of 1.8 V–3.3 V; If the package does not have a dedicated VCCD pin, it is internally connected to VCCA. Refer to the Hardware Design Guide for details.
39	VDD15R	AI	RF power supply, 1.8 V
38	VDD15L	AI	RF LO power supply, 1.8 V
37	VDD15O	AO	Internal LDO output power, sourced from VCCA; supplies VDD15L and VDD15R at 1.5 V

22	VCAM	AO	Internal LDO output; supports 2.5 V–3.25 V or 3.3 V when used as internal power output
60	VCMAU	AO	Internal reference output; no load drive capability
59	VCCAU33	AI	Audio module power supply input, 3.3 V, or connected to VCAM (2.8 V–3.3 V)
56	VCCAU27	AO	Audio module power supply; supports internal 2.7 V output for external analog MIC bias supply
63	AGND	AI	Audio analog ground
61	LOUT_P	AO	Audio DAC output, positive terminal
62	LOUT_N	AO	Audio DAC output, negative terminal
57	MIC_P	AI	Microphone input, positive terminal
58	MIC_N	AI	Microphone input, negative terminal
35	XI	AI	High-speed crystal oscillator input
36	XO	AO	High-speed crystal oscillator output
40	ANT	AI/O	RF antenna port
GND	EPAD	AI	Ground

Notes:

1) **I/Os in the VCC1/VCC18 power domain are in a high-impedance input state only when powered.**
2) **Comparator inputs can be compared against an internal reference voltage or an I/O reference voltage.**
3) **Only one I/O can be selected as a wake-up source within the same wake-up group.**

Table 1-7-1-2: GPIO Pin Analog Function Table

Pin Name	I/O Type	Description Default State	Power Domain	Wake-up I/O Group	ADC Channel (any-terminal sampling)	Comparator Channel (P/N terminal comparison)	Special Function
HSDP	AI/O	USB DP	VCC				Digital I/O: PC6
HSDM	AI/O	USB DM	VCC				Digital I/O: PC7
PA0	I/O	Hi-Z Input	VCC	Wake-up I/O Group 0 Wake-up I/O Group 1	ADKEY_CHANNEL3		Low-Power PWM0 MIPI_CSI1_1P
PA1	I/O	Hi-Z Input	VCC	Wake-up I/O Group 2 Wake-up I/O Group 3			Low-Power PWM1 MIPI_CSI1_1N
PA2	I/O	Hi-Z Input	VCC	Wake-up I/O Group 4			MIPI_CSI0_0P

PA3	I/O	Hi-Z Input	VCC	Wake-up I/O Group 5			MIPI_CSI0_0N
PA4	I/O	Hi-Z Input	VCC				MIPI_CSI0_1P
PA5	I/O	Hi-Z Input	VCC				MIPI_CSI0_1N
PA6	I/O	Hi-Z Input	VCC		ADKEY_CHANNEL1	PIRVIN_P1	Low-Power PWM0 Low-Speed Crystal Oscillator Output DCFB Output
PA7	I/O	Hi-Z Input	VCC		ADKEY_CHANNEL2	PIRVIN_P2	Low-Power PWM1 Low-Speed Crystal Oscillator Input DC33FB Output
PA8	I/O	Hi-Z Input	VCC			PIRVIN_P2	Low-Power PWM2
PA9	I/O	100k PU Input	VCC			VREFPIR_N2	Low-Power PWM2
PA10	I/O	100k PU Input	VCC			VREFPIR_N1	Low-Power PWM3
PA11	I/O	Hi-Z Input	VCC		ADKEY_CHANNEL1	PIRVIN_P1	Low-Power PWM3
PA12	I/O	Hi-Z Input	VCC			PIRVIN_P1	
PA13	I/O	Hi-Z Input	VCC			PIRVIN_P1	
PA14	I/O	Hi-Z Input	VCC			PIRVIN_P1	
PA15	I/O	Hi-Z Input	VCC	Wake-up I/O Group 1 Wake-up I/O Group 5	ADKEY_CHANNEL2	PIRVIN_P2	Low-Power PWM2
PD0	I/O	Hi-Z Input	VCC	Wake-up I/O Group 1 Wake-up I/O Group 3 Wake-up I/O Group 5	ADKEY_CHANNEL3		Low-Power PWM1 MIPI_CSI1_0N
PD1	I/O	Hi-Z Input	VCC				Low-Power PWM0 MIPI_CSI1_0P
PD2	I/O	Hi-Z Input	VCC				MIPI_DSI_0N
PD3	I/O	Hi-Z Input	VCC				MIPI_DSI_0P
PD4	I/O	Hi-Z Input	VCC				MIPI_DSI_1N
PD5	I/O	Hi-Z Input	VCC				MIPI_DSI_1P
PD6	I/O	Hi-Z Input	VCC				MIPI_DSI_2N
PD7	I/O	Hi-Z Input	VCC				MIPI_DSI_2P
PD12	I/O	Hi-Z Input	VCC				Low-Power PWM0 USB11_DM DCFB Output
PD13	I/O	Hi-Z Input	VCC				Low-Power PWM1 USB11_DP DC33FB Output
PB6	I/O	Hi-Z Input	VCC1	Wake-up I/O Group 0 Wake-up I/O Group 2 Wake-up I/O Group 4	ADKEY_CHANNEL6		
PB7	I/O	Hi-Z Input	VCC1				
PB8	I/O	Hi-Z Input	VCC1				
PB9	I/O	Hi-Z Input	VCC1				
PB10	I/O	Hi-Z Input	VCC1				
PB11	I/O	Hi-Z Input	VCC1				

PB12	I/O	Hi-Z Input	VCC1				
PB13	I/O	Hi-Z Input	VCC1				
PB15	I/O	Hi-Z Input	VCC1				
PB14	I/O	Hi-Z Input	VCC1	Wake-up I/O Group 0 Wake-up I/O Group 2 Wake-up I/O Group 4 Wake-up I/O Group 5			
PC0	I/O	Hi-Z Input	VCC1	Wake-up I/O Group 0 Wake-up I/O Group 1			
PC1	I/O	Hi-Z Input	VCC1	Wake-up I/O Group 2 Wake-up I/O Group 4			
PC2	I/O	Hi-Z Input	VCC1	Wake-up I/O Group 0 Wake-up I/O Group 2 Wake-up I/O Group 4 Wake-up I/O Group 5			
PC8	I/O	Hi-Z Input	VCC_SD		ADKEY_CHANNEL4		
PC9	I/O	Hi-Z Input	VCC_SD				
PC10	I/O	Hi-Z Input	VCC_SD				
PC11	I/O	Hi-Z Input	VCC_SD				
PC12	I/O	Hi-Z Input	VCC_SD				
PB0	I/O	Hi-Z Input	VCC_FLS				
PB1	I/O	Hi-Z Input	VCC_FLS				
PB2	I/O	Hi-Z Input	VCC_FLS				
PB3	I/O	Hi-Z Input	VCC_FLS				
PB4	I/O	Hi-Z Input	VCC_FLS				
PB5	I/O	Hi-Z Input	VCC_FLS				
PC14	I/O	Hi-Z Input	VCC18		ADKEY_CHANNEL5		
PC15	I/O	Hi-Z Input	VCC18				
PD14	I/O	Hi-Z Input	VCC18				
PD15	I/O	Hi-Z Input	VCC18				
PE0	I/O	Hi-Z Input	VCC18				

1.7.2. Digital Pin Functions

Table 1-7-2-1: GPIO Pin Digital Function Table

Pin Name	I/O Type	Description Default State	Power Domain	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA0	I/O	Hi-Z Input	VCC		qspi_io3	rmii_crs_dv	
PA1	I/O	Hi-Z Input	VCC		qspi_io2	rmii_tx_en	
PA2	I/O	Hi-Z Input	VCC		qspi_io1	rgmii_rxd2	
PA3	I/O	Hi-Z Input	VCC		qspi_io0	rgmii_rxd3	
PA4	I/O	Hi-Z Input	VCC		qspi_cs0	rgmii_txd2	
PA5	I/O	Hi-Z Input	VCC		qspi_clk	rgmii_txd3	
PA6	I/O	Hi-Z Input	VCC		qspi_clk	rmii_txd1	
PA7	I/O	Hi-Z Input	VCC		qspi_io0	rmii_txd0	
PA8	I/O	Hi-Z Input	VCC		qspi_io1		
PA9	I/O	100k PU Input	VCC		qspi_io2	rmii_ref_clkin	
PA10	I/O	100k PU Input	VCC		qspi_io3	rmii_rxd1	
PA11	I/O	Hi-Z Input	VCC		qspi_io2		
PA12	I/O	Hi-Z Input	VCC				
PA13	I/O	Hi-Z Input	VCC				
PA14	I/O	Hi-Z Input	VCC				
PA15	I/O	Hi-Z Input	VCC		qspi_io3	rmii_rxd0	
PB0	I/O	Hi-Z Input	VCC_FLS				
PB1	I/O	Hi-Z Input	VCC_FLS				
PB2	I/O	Hi-Z Input	VCC_FLS				
PB3	I/O	Hi-Z Input	VCC_FLS				
PB4	I/O	Hi-Z Input	VCC_FLS				
PB5	I/O	Hi-Z Input	VCC_FLS				
PB6	I/O	Hi-Z Input	VCC1	rgmii_rxd2	dvp_vsync	bt_vsync	
PB7	I/O	Hi-Z Input	VCC1	rgmii_rxd3	dvp_hsync	bt_hsync	
PB8	I/O	Hi-Z Input	VCC1	rmii_rxd0	dvp_data_in7	bt_dat7	lcd_te
PB9	I/O	Hi-Z Input	VCC1	rmii_rxd1	dvp_mclk	bt_blank_o	lcd_te
PB10	I/O	Hi-Z Input	VCC1	rmii_ref_clkin	dvp_data_in6	bt_dat6	

PB11	I/O	Hi-Z Input	VCC1	rmii_txd0	dvp_data_in5	bt_dat5	
PB12	I/O	Hi-Z Input	VCC1	rmii_txd1	dvp_pixel_clk_in	bt_pixel_clk	
PB13	I/O	Hi-Z Input	VCC1	rmii_tx_en	dvp_data_in4	bt_dat4	
PB14	I/O	Hi-Z Input	VCC1	rmii_crs_dv	dvp_data_in0	bt_dat0	
PB15	I/O	Hi-Z Input	VCC1	rmii_rx_er	dvp_data_in3	bt_dat3	rgmii_txc
PC0	I/O	Hi-Z Input	VCC1	rgmii_txd2	dvp_data_in1	bt_dat1	
PC1	I/O	Hi-Z Input	VCC1	rgmii_txd3	dvp_data_in2	bt_dat2	
PC2	I/O	Hi-Z Input	VCC1		dvp_data_in8	lcd_te	
PC6	I/O	Hi-Z Input	VCC				
PC7	I/O	Hi-Z Input	VCC				
PC8	I/O	Hi-Z Input	VCC_SD		rmii_rxd0		
PC9	I/O	Hi-Z Input	VCC_SD		rmii_rxd1		
PC10	I/O	Hi-Z Input	VCC_SD	bt_vsync	rmii_ref_clkin		
PC11	I/O	Hi-Z Input	VCC_SD	bt_hsync	rmii_txd0		
PC12	I/O	Hi-Z Input	VCC_SD	bt_dat7	rmii_txd1	lcd_dotclk_or_rwr	
PC14	I/O	Hi-Z Input	VCC18	bt_dat6	rmii_crs_dv		
PC15	I/O	Hi-Z Input	VCC18	bt_dat5	rmii_rx_er	rgmii_txc	
PD0	I/O	Hi-Z Input	VCC	rgmii_txc		rmii_rx_er	rgmii_rxd2
PD1	I/O	Hi-Z Input	VCC				rgmii_rxd3
PD2	I/O	Hi-Z Input	VCC	bt_vsync			rmii_rxd0
PD3	I/O	Hi-Z Input	VCC	bt_hsync			rmii_rxd1
PD4	I/O	Hi-Z Input	VCC	bt_dat7			rmii_ref_clkin
PD5	I/O	Hi-Z Input	VCC	bt_blank_o			rmii_txd0
PD6	I/O	Hi-Z Input	VCC	bt_dat6			rmii_txd1
PD7	I/O	Hi-Z Input	VCC	bt_dat5			rmii_tx_en
PD12	I/O	Hi-Z Input	VCC	bt_dat1			lcd_te
PD13	I/O	Hi-Z Input	VCC	bt_dat2			lcd_te
PD14	I/O	Hi-Z Input	VCC18	bt_pixel_clk	rgmii_rxd2	lcd_hsync_or_dc	
PD15	I/O	Hi-Z Input	VCC18	bt_dat4	rgmii_rxd3	dvp_vsync	
PE0	I/O	Hi-Z Input	VCC18	bt_dat0	rgmii_txd2	lcd_vsync_or_cs	

1.7.3. GPIO Output Arbitrary Mapping Functions

Table 1-7-3-1: GPIO Output Arbitrary Mapping Table

No.	Function Name	Function Description
1	CLK_TO_IO	Clock output to I/O
2	PDM_MCLK	PDM MCLK output
3	DUAL_ORG_FSYNC	DUAL_ORG_FSYNC output
4	DAC_PDM_OUT	DAC module PDM output
5	DVP_MCLK_OUT	DVP module MCLK output
6	PA_EN	External PA enable signal
7	ANTENNA_SEL	Dual-antenna selection signal
8	COMP_DOUT_DIG1	Comparator 0 digital I/O output
9	COMP_DOUT_DIG0	Comparator 1 digital I/O output
10	SPI2_IO3_OUT	SPI2 DATA output 3
11	SPI2_IO2_OUT	SPI2 DATA output 2
12	SPI2_IO1_OUT	SPI2 DATA output 1
13	SPI2_IO0_OUT	SPI2 DATA output 0
14	SPI2_SCK_OUT	SPI2 SCLK output
15	SPI2_NSS_OUT	SPI2 NSS output
16	SPI1_IO3_OUT	SPI1 DATA output 3
17	SPI1_IO2_OUT	SPI1 DATA output 2
18	SPI1_IO1_OUT	SPI1 DATA output 1
19	SPI1_IO0_OUT	SPI1 DATA output 0
20	SPI1_NSS_OUT	SPI1 NSS output
21	SPI1_SCK_OUT	SPI1 SCK output
22	SPI0_IO3_OUT	SPI0 DATA output 3
23	SPI0_IO2_OUT	SPI0 DATA output 2
24	SPI0_IO1_OUT	SPI0 DATA output 1
25	SPI0_IO0_OUT	SPI0 DATA output 0
26	SPI0_SCK_OUT	SPI0 SCK output
27	SPI0_NSS_OUT	SPI0 NSS output
28	LCD_DE_OR_ERD	LCD display interface DE/ERD output
29	LCD_HSYNC_OR_DC	LCD display interface HSYNC/DC output

30	LCD_VSYNC_OR_CS	LCD display interface VSYNC/CS output
31	LCD_DOTCLK_OR_RWR	LCD display interface DOTCLK/RWR output
32	LCD_DATA_O[23]	LCD display interface data bit output [23]
33	LCD_DATA_O[22]	LCD display interface data bit output [22]
34	LCD_DATA_O[21]	LCD display interface data bit output [21]
35	LCD_DATA_O[20]	LCD display interface data bit output [20]
36	LCD_DATA_O[19]	LCD display interface data bit output [19]
37	LCD_DATA_O[18]	LCD display interface data bit output [18]
38	LCD_DATA_O[17]	LCD display interface data bit output [17]
39	LCD_DATA_O[16]	LCD display interface data bit output [16]
40	LCD_DATA_O[15]	LCD display interface data bit output [15]
41	LCD_DATA_O[14]	LCD display interface data bit output [14]
42	LCD_DATA_O[13]	LCD display interface data bit output [13]
43	LCD_DATA_O[12]	LCD display interface data bit output [12]
44	LCD_DATA_O[11]	LCD display interface data bit output [11]
45	LCD_DATA_O[10]	LCD display interface data bit output [10]
46	LCD_DATA_O[9]	LCD display interface data bit output [9]
47	LCD_DATA_O[8]	LCD display interface data bit output [8]
48	LCD_DATA_O[7]	LCD display interface data bit output [7]
49	LCD_DATA_O[6]	LCD display interface data bit output [6]
50	LCD_DATA_O[5]	LCD display interface data bit output [5]
51	LCD_DATA_O[4]	LCD display interface data bit output [4]
52	LCD_DATA_O[3]	LCD display interface data bit output [3]
53	LCD_DATA_O[2]	LCD display interface data bit output [2]
54	LCD_DATA_O[1]	LCD display interface data bit output [1]
55	LCD_DATA_O[0]	LCD display interface data bit output [0]
56	IIS0_DO	IIS0 DAT output
57	IIS0_BCLK_OUT	IIS0 BCLK output
58	IIS0_WSCLK_OUT	IIS0 WS output
59	IIS0_MCLK_OUT	IIS0 MCLK output
60	IIS1_MCLK_OUT	IIS1 MCLK output
61	IIS1_DO	IIS1 DAT output
62	IIS1_BCLK_OUT	IIS1 BCLK output
63	IIS1_WSCLK_OUT	IIS1 WS output

64	IO2IO_CHANNAL0	I/O-to-I/O channel 0 output
65	IO2IO_CHANNAL1	I/O-to-I/O channel 1 output
66	IO2IO_CHANNAL2	I/O-to-I/O channel 2 output
67	IO2IO_CHANNAL3	I/O-to-I/O channel 3 output
68	SDHOST_DAT3_OUT	SDHOST0 DAT3 output
69	SDHOST_DAT2_OUT	SDHOST0 DAT2 output
70	SDHOST_DAT1_OUT	SDHOST0 DAT1 output
71	SDHOST_DAT0_OUT	SDHOST0 DAT0 output
72	SDHOST_CMD_OUT	SDHOST0 CMD output
73	SDHOST_SCLK_O	SDHOST0 SDCLK output
74	SDHOST1_DAT3_OUT	SDHOST1 DAT3 output
75	SDHOST1_DAT2_OUT	SDHOST1 DAT2 output
76	SDHOST1_DAT1_OUT	SDHOST1 DAT1 output
77	SDHOST1_DAT0_OUT	SDHOST1 DAT0 output
78	SDHOST1_SCLK_O	SDHOST1 SDCLK output
79	SDHOST1_CMD_OUT	SDHOST1 CMD output
80	QSPI_NSS1_OUT	QSPI module CS1 output
81	OSPI_CS_IO	OSPI module CS output
82	LED_TMR3_PWM_OUT	LED Timer3 PWM output
83	LED_TMR2_PWM_OUT	LED Timer2 PWM output
84	LED_TMR1_PWM_OUT	LED Timer1 PWM output
85	LED_TMR0_PWM_OUT	LED Timer0 PWM output
86	TMR0_PWM_OUT	Timer0 PWM output
87	TMR1_PWM_OUT	Timer1 PWM output
88	TMR2_PWM_OUT	Timer2 PWM output
89	TMR3_PWM_OUT	Timer3 PWM output
90	STMR5_PWM_OUT	Simple timer5 PWM output
91	STMR4_PWM_OUT	Simple timer4 PWM output
92	STMR3_PWM_OUT	Simple timer3 PWM output
93	STMR2_PWM_OUT	Simple timer2 PWM output
94	STMR1_PWM_OUT	Simple timer1 PWM output
95	STMR0_PWM_OUT	Simple timer0 PWM output
96	UART6_TX	UART6 output TX output
97	UART5_TX	UART5 output TX output

98	UART4_TX	UART4 output TX output
99	UART1_OUT	UART1 output TX output
100	UART1_CTS_DE_OUT	UART1 output CTS_DE output
101	UART1_RTS_RE_O	UART1 output RTS_RE output
102	UART0_OUT	UART0 output TX output
103	UART0_CTS_DE_OUT	UART0 output CTS_DE output
104	UART0_RTS_RE_O	UART0 output RTS_RE output
105	GRANT_WIFI_SWITCH_O	Bluetooth coexistence Wi-Fi switch signal
106	GRANT_BT_SWITCH_O	Bluetooth coexistence switch signal
107	GRANT_BT	Bluetooth coexistence BT arbitration signal
108	RF_PA_EN_FEM	External RF FEM PA enable signal
109	RF_TRX_SW_FEM	External RF TX/RX selection signal
110	RF_SWITCH_EN0	External RF switch enable 0
111	RF_RX_EN_FEM	External RF FEM receive enable
112	RF_SWITCH_EN1	External RF switch enable 1
113	RF_TX_EN_FEM	External RF FEM transmit enable
114	RF_EXT_LNA_EN	External RF LNA enable signal

1.7.4. GPIO Input Arbitrary Mapping Functions

Table 1-7-4-1: GPIO Input Arbitrary Mapping Table

No.	Function Name	Function Description
1	IO2IO_CHANNAL0_PRE	I/O-to-I/O arbitrary mapping channel 0 input
2	IO2IO_CHANNAL1_PRE	I/O-to-I/O arbitrary mapping channel 1 input
3	IO2IO_CHANNAL2_PRE	I/O-to-I/O arbitrary mapping channel 2 input
4	IO2IO_CHANNAL3_PRE	I/O-to-I/O arbitrary mapping channel 3 input
5	LCD_DATA_I[0]	LCD display module data input [0]
6	LCD_DATA_I[1]	LCD display module data input [1]
7	LCD_DATA_I[2]	LCD display module data input [2]
8	LCD_DATA_I[3]	LCD display module data input [3]
9	LCD_DATA_I[4]	LCD display module data input [4]
10	LCD_DATA_I[5]	LCD display module data input [5]
11	LCD_DATA_I[6]	LCD display module data input [6]

12	LCD_DATA_I[7]	LCD display module data input [7]
13	LCD_DATA_I[8]	LCD display module data input [8]
14	LCD_DATA_I[9]	LCD display module data input [9]
15	LCD_DATA_I[10]	LCD display module data input [10]
16	LCD_DATA_I[11]	LCD display module data input [11]
17	LCD_DATA_I[12]	LCD display module data input [12]
18	LCD_DATA_I[13]	LCD display module data input [13]
19	LCD_DATA_I[14]	LCD display module data input [14]
20	LCD_DATA_I[15]	LCD display module data input [15]
21	LCD_DATA_I[16]	LCD display module data input [16]
22	LCD_DATA_I[17]	LCD display module data input [17]
23	LCD_DATA_I[18]	LCD display module data input [18]
24	LCD_DATA_I[19]	LCD display module data input [19]
25	LCD_DATA_I[20]	LCD display module data input [20]
26	LCD_DATA_I[21]	LCD display module data input [21]
27	LCD_DATA_I[22]	LCD display module data input [22]
28	LCD_DATA_I[23]	LCD display module data input [23]
29	LCD_TE_ANY_MAP	LCD display module TE input
30	TMR0_SYNCI_IO	IR Timer0 input
31	TMR0_CAP_PIN	normal timer0 CAP and external count input
32	TMR1_CAP_PIN	IR timer1 CAP and external count input
33	TMR2_CAP_PIN	IR timer2 CAP and external count input
34	TMR3_CAP_PIN	normal timer3 CAP and external count input
35	STMR0_CAP_PIN	sample timer0 CAP and external count input
36	STMR1_CAP_PIN	sample timer1 CAP and external count input
37	STMR2_CAP_PIN	sample timer2 CAP and external count input
38	STMR3_CAP_PIN	sample timer3 CAP and external count input
39	STMR4_CAP_PIN	sample timer4 CAP and external count input
40	STMR5_CAP_PIN	sample timer5 CAP and external count input
41	SPI0_NSS_IN	SPI0 module NSS input
42	SPI0_SCK_IN	SPI0 module SCK input
43	SPI0_IO0_IN	SPI0 module data input 0
44	SPI0_IO1_IN	SPI0 module data input 1
45	SPI0_IO2_IN	SPI0 module data input 2

46	SPI0_IO3_IN	SPI0 module data input 3
47	SPI1_NSS_IN	SPI1 module NSS input
48	SPI1_SCK_IN	SPI1 module SCK input
49	SPI1_IO0_IN	SPI1 module data input 0
50	SPI1_IO1_IN	SPI1 module data input 1
51	SPI1_IO2_IN	SPI1 module data input 2
52	SPI1_IO3_IN	SPI1 module data input 3
53	SPI2_NSS_IN	SPI2 module NSS input
54	SPI2_SCK_IN	SPI2 module SCK input
55	SPI2_IO0_IN	SPI2 module data input 0
56	SPI2_IO1_IN	SPI2 module data input 1
57	SPI2_IO2_IN	SPI2 module data input 2
58	SPI2_IO3_IN	SPI2 module data input 3
59	SDHOST_CMD_IN	SDHOST0 CMD input
60	SDHOST_DAT0_IN	SDHOST0 DAT0 input
61	SDHOST_DAT1_IN	SDHOST0 DAT1 input
62	SDHOST_DAT2_IN	SDHOST0 DAT2 input
63	SDHOST_DAT3_IN	SDHOST0 DAT3 input
64	SDHOST1_CMD_IN	SDHOST1 CMD input
65	SDHOST1_DAT0_IN	SDHOST1 DAT0 input
66	SDHOST1_DAT1_IN	SDHOST1 DAT1 input
67	SDHOST1_DAT2_IN	SDHOST1 DAT2 input
68	SDHOST1_DAT3_IN	SDHOST1 DAT3 input
69	UART0_IN	UART0 RX input
70	UART0_CTS_DE_IN	UART0 CTS/DE input
71	UART1_IN	UART1 RX input
72	UART1_CTS_DE_IN	UART1 CTS/DE input
73	UART4_RX	UART4 RX input
74	UART5_RX	UART5 RX input
75	UART6_RX	UART6 RX input
76	IIS0_MCLK_IN	IIS0 module MCLK input
77	IIS0_WSCLK_IN	IIS0 module WSCLK input
78	IIS0_BCLK_IN	IIS0 module BCLK input
79	IIS0_DI	IIS0 module data input (DI)

80	IIS1_MCLK_IN	IIS0 module MCLK input
81	IIS1_WSCLK_IN	IIS0 module WSCLK input
82	IIS1_BCLK_IN	IIS0 module BCLK input
83	IIS1_DI	IIS0 module data input (DI)
84	PDM_DATA	PDM DATA input
85	PTA_REQ	PTA REQ input
86	PTA_PRI	PTA PRI input
87	FREQ_IND	FREQ IND input
88	EXT_RFSWITCH_EN0_IN	External RF switch enable 0 input
89	EXT_RF_PA_EN_IN_PRE	EXT_PA enable input

2. Functional Description

2.1. Wi-Fi + BLE + SLE

The TXW828-E016FL supports 2.4 GHz Wi-Fi, BLE, and SLE, integrating an IEEE 802.11 b/g/n baseband and RF (Radio Frequency) circuit, including a power amplifier (PA), low noise amplifier (LNA), RF balun, antenna switch, and power management module.

The TXW828-E016FL Wi-Fi baseband implements Orthogonal Frequency Division Multiplexing (OFDM) technology and is backward compatible with Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) technologies, supporting the IEEE 802.11 b/g/n protocol. Supports 20/40 MHz standard bandwidth and 5/10 MHz narrow bandwidth, providing a maximum physical layer rate of 150 Mbit/s.

- Supports IEEE 802.11 b/g/n standard and 20/40 MHz channel bandwidth
- Integrated PA, LNA, and RX/TX switch, reducing BOM cost
- Supports STA, AP, and hardware AP+STA operating modes; supports up to 10 STAs in AP mode
- Supports frame aggregation (TX/RX A-MPDU, RX A-MSDU)
- Supports PS-Poll and U-APSD power-saving functions
- Supports WPA/WPA2/WPA3
- Compatible with 802.11n Legacy mode, Mixed mode, and Green Field mode
- Supports 802.11n Short-GI and Long-GI
- Space Time Block Coding (STBC)
- Supports 1T1R mode; data rate up to 150 Mbps
- Supports Wi-Fi Multimedia (WMM)
- Supports Immediate Block ACK and Delayed Block ACK
- Supports fragmentation and defragmentation

- Supports automatic beacon monitoring (hardware TSF)
- Supports SLE 1/2/4 MHz bandwidth
- Supports Bluetooth LE network provisioning
- Supports external PA and external LNA

2.2. Processor and Memory

2.2.1. CPU

The TXW828-E016FL integrates one XuanTie E804FD (CPU0) and one XuanTie E804D (CPU1), with a maximum operating frequency of 240 MHz. Key features are as follows:

- Reduced Instruction Set Computer (RISC) architecture
- 32-bit data with 16-bit/32-bit mixed-length instruction encoding
- Supports single-precision floating-point operations (CPU0 only)
- Supports DSP instructions
- 3-stage pipeline
- 32 KB cache
- Single-cycle hardware multiplier
- Vectored Interrupt Controller (VIC) and SysTick timer
- Interrupt response latency of only 13 processor cycles

2.2.2. Memory

The TXW828-E016FL on-chip memory includes:

- ROM: Bootloader and partial kernel functions
- 368 KB SRAM (expandable up to 560 KB by powering down select modules)
- 64-bit eFuse: for key storage and customer-defined use

2.2.3. Memory Expansion

The TXW828-E016FL supports memory expansion via the SPI interface, including SPI Flash and PSRAM (PSRAM is built-in). The on-chip QSPI controller supports external QSPI Flash and PSRAM (up to two memory devices), with XIP support. QSPI supports address space mapping for up to 256 MB of external Flash and PSRAM; supports 1.8 V and 3.3 V Flash and DTR mode. The on-chip OSPI controller supports external PSRAM with address space mapping of up to 128 MB.

2.3. System Clock

The TXW828-E016FL supports the following clock sources:

- 128 kHz LIRC
- 40 kHz always-on RC
- 8 MHz HIRC
- 32.768 kHz low-speed crystal oscillator
- 24–50 MHz high-speed crystal oscillator
- 480 MHz fractional-divider USB 2.0 PLL
- External I/O clock input source

2.4. Analog Peripherals

2.4.1. Analog-to-Digital Converter (SAR ADC)

The TXW828-E016FL integrates one 11-bit SAR ADC operating in ADC mode. Key features are as follows:

- The ADC has 8 sampling channels, including 2 priority channels and 6 non-priority channels.
- Non-priority channel data supports both CPU read and DMA access; priority channel data supports CPU read only.

- Supports single-channel mode and multi-channel scan mode
- Sampling rate up to 1 Msps
- Supports 10-bit ADC conversion resolution
- Supports ADC conversion triggered by basic timers 0/1/2/3, simple timers 0/1/2/3/4/5, and software
- Supports sampling channels for external I/O, internal temperature sensor, and supply voltage.

2.4.2. Analog Comparator (CMP)

The TXW828-E016FL integrates two analog comparators.

- Supports voltage comparison between two I/O pins
- Supports comparator result output to I/O
- Supports low-power mode wake-up

2.4.3. Temperature Sensor

The TXW828-E016FL integrates one temperature sensor. The sensor voltage is sampled via an internal ADC channel and converted to the chip's internal temperature value through calculation.

2.4.4. USB2.0 PHY

The TXW828-E016FL integrates a USB 2.0 PHY which, together with the USB 2.0 SIE, supports HS/FS transfers.

The high-performance USB 2.0 HS PHY incorporates a proprietary CDR architecture, ensuring reliable operation in harsh environments. High-speed mode is supported without an external USB 2.0 PHY, with a theoretical transfer rate of up to 480 Mbps. When USB 2.0 functionality is not required, the pins can be used as two GPIOs.

2.4.5. MIPI DPHY RX

The TXW828-E016FL integrates a MIPI DPHY RX compatible with version 1.1, used in conjunction with the MIPI CSI2 HOST.

The MIPI DPHY RX provides 4 differential lane pairs, each supporting 80 Mbps to 1.5 Gbps. Lane order and polarity are freely adjustable for convenient PCB routing; all lanes support LP-RX and HS-RX. When MIPI DPHY RX functionality is not required, the pins can be used as GPIOs.Below are classic scenarios for MIPI RX usage:

Application	CLK	DATA	CLK	DATA
1 Lane Sensor * 1	PA2/3	PA4/5		
1 Lane Sensor * 2	PA2/3	PA4/5	PD0/1	PA0/1
2 Lane Sensor * 1	PA2/3	PA4/5		PA0/1

2.4.6. MIPI DPHY TX

The TXW828-E016FL integrates a MIPI DPHY TX compatible with version 1.1, used in conjunction with the MIPI DSI HOST.

The MIPI DPHY TX provides 3 differential lane pairs, each supporting 960/480/320/240/160/96/80 Mbps. Lane order and polarity are freely adjustable for convenient PCB routing; all lanes support LP-TX, LP-RX, LP-CD, and HS-TX. When MIPI DPHY TX functionality is not required, the pins can be used as GPIOs.

2.4.7. XOSC

The TXW828-E016FL integrates one high-speed crystal oscillator circuit, requiring an external passive crystal oscillator of 24–50 MHz.

2.4.8. PLL

The TXW828-E016FL integrates a high-performance 480 MHz fractional-divider USB 2.0 PLL.

2.4.9. Audio ADC

The TXW828-E016FL integrates one delta-sigma audio ADC with a built-in PGA, supporting both single-ended and differential analog microphone inputs.

- Audio ADC supports sample rates of 8/11.025/12/16/22.05/24/32/44.1/48 kHz
- Supports single-ended and differential-input high-performance analog MIC with built-in PGA
- Supports VAD (Voice Activity Detection) event generation

2.4.10. Audio DAC

The TXW828-E016FL integrates one delta-sigma audio DAC.

- Audio DAC supports sample rates of 8/11.025/12/16/22.05/24/32/44.1/48/96 kHz
- Supports one-bit DAC output
- Supports 10-band adjustable EQ
- Supports fade-in/fade-out volume control
- Supports DRC with two configurable knee points

2.5. Digital Peripherals

2.5.1. GPIO

The TXW828-E016FL integrates up to 57 general-purpose GPIOs. Key features are as follows:

- Pull-up resistance is configurable; available values: 4.7 kΩ and 100 kΩ
- Pull-down resistance: 100 kΩ
- Supports 4-level configurable I/O output drive strength: 4/8/16/20 mA; PB12/PD14 are high-speed I/Os with a configurable range of 8/20/32/44 mA

- Supports push-pull and open-drain output
- Supports I/O state latch after power-off in low-power mode
- Supports I/O state latch under always-on power: PA[6:15]
- Supports level- and edge-triggered interrupt and wake-up on any I/O
- Supports ADC analog input function
- Supports independent enable control for digital I/O input and output directions; digital I/O input/output can be disabled independently
- Supports input hysteresis

2.5.2. SPI/IIC

The TXW828-E016FL integrates three SPI controllers. SPI0/1/2 all support master and slave modes; SPI1/2 each support either SPI or I2C function (mutually exclusive). Key features are as follows:

SPI features:

- Supports master and slave modes
- Supports Motorola SPI
- Supports master/slave half-duplex transceiving
- Programmable serial clock polarity and phase
- Supports 4 operating modes:
  - Standard mode: SCLK, CS, IO0 (MOSI), IO1 (MISO); 1 bit per SCLK cycle
  - 3-wire mode: SCLK, CS, IO0; 1 bit per SCLK cycle
  - Dual mode: SCLK, CS, IO0, IO1; 2 bits per SCLK cycle
  - Quad mode: SCLK, CS, IO0, IO1, IO2, IO3; 4 bits per SCLK cycle
- Transfer completion flag with MCU interrupt
- Supports master mode baud rate up to 1/2 of the system clock
- Supports slave mode baud rate up to 1/2 of the system clock
- Supports selectable data width of 1 to 32 bits

- Supports DMA (Direct Memory Access)
- Supports MSB-first or LSB-first transmission

I2C features:

- Supports master and slave modes
- Supports master clock synchronization and arbitration
- Supports slave SCL clock stretching when transmit data is not ready or receive buffer is full
- Supports 7-bit and 10-bit slave addressing
- Supports DMA
- Supports SMBUS
- Supports SMBUS ALERT
- Supports SMBUS HOST ADDRESSS
- Supports SMBUS DEVICE DEFAULT ADDRESS
- Supports SMBUS ALERT RESPONSE ADDRESS
- Supports timeout detection

2.5.3. UART

The TXW828-E016FL integrates five UART controllers: three basic-function UARTs (UART4/5/6) and two full-function UARTs (UART0/1).

UART0/1 features:

- Supports 8-bit and 9-bit data modes
- Supports parity check
- 4-frame receive buffer and 1-frame transmit buffer
- Supports RX and TX DMA
- Supports hardware flow control; RTS_N and CTS_N each have independent enable signals; RTS_N can be configured to assert after N (N = 0, 1, 2, 3) bytes are received in the buffer
- Hardware receive timeout detection; configurable timeout range: 1 to

65536 baud periods

- Supports RS-485 mode

UART4/5/6 features:

- Supports half-duplex operation
- Supports 9-bit data transmission
- Supports software parity check
- Supports DMA

2.5.4. IIS_PCM

The TXW828-E016FL integrates two IIS_PCM modules for extended audio functionality. Key features are as follows:

- Supports I2S, left-justified, right-justified, and PCM format transmission
- Supports left-channel, right-channel, and stereo modes
- Supports master and slave modes
- Supports 2 to 32-bit data width
- Supports MCLK output mode; also supports using an input MCLK as the master/slave clock source
- Supports left/right channel swap
- Supports automatic dual-address switching
- IIS0 supports single-wire SPI mode

2.5.5. PDM

The TXW828-E016FL integrates one PDM module for extended audio functionality. The PDM module is an audio interface for digital MEMS microphones, providing a configurable high-precision output clock and supporting left-channel, right-channel, and stereo operation. The integrated PDM interface features are as follows:

- Supports conversion of PDM data from digital MEMS microphone input to

16-bit PCM data

- Supports left-channel, right-channel, and stereo modes
- Provides decimation ratios of 50, 100, and 200 for PDM/PCM mode
- Supports left/right channel swap
- Supports DMA automatic dual-address switching

2.5.6. CORDIC Accelerator

The TXW828-E016FL integrates one CORDIC accelerator module.

- Supports 16-bit sine and cosine computation in rotation mode.

2.5.7. USB1.1 SIE

The TXW828-E016FL integrates a USB 1.1 SIE Controller, compliant with the standard USB 1.1 Full-Speed Host and Device protocol.

- Supports control transfers on Endpoint 0
- Supports bulk, interrupt, and isochronous transfers on Endpoints 1–3

2.5.8. USB2.0 SIE

The TXW828-E016FL integrates a USB 2.0 SIE Controller, compliant with the standard USB 2.0 High-Speed and Full-Speed Host and Device protocol.

- Supports control transfers on Endpoint 0
- Supports bulk, interrupt, and isochronous transfers on Endpoints 1–6

2.5.9. MIPI CSI2 HOST

The TXW828-E016FL integrates two MIPI CSI2 HOST interface modules for connecting external cameras. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports two 1-data-lane MIPI CSI2 HOST interfaces

- Supports one 2-data-lane MIPI CSI2 HOST interface
- Supports cropping
- Supports multiple virtual channel inputs

2.5.10. Camera DVP Interface

The TXW828-E016FL integrates one CMOS sensor DVP interface module for connecting external cameras. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports sensor parallel interface
- Supports HSYNC and VSYNC polarity selection
- Supports HSYNC and VSYNC invalid detection
- Supports VSYNC recovery function to save I/O pins
- Supports data formats: YUV422 and RAW8/10/12 DATA

2.5.11. PARALLEL_IN

The TXW828-E016FL integrates one PARALLEL_IN interface module for receiving BT.601, BT.656, and BT.1120 format data from analog cameras. Key features are as follows:

- Supports progressive scan data reception in BT.601, BT.656, and BT.1120 formats
- Supports maximum resolution of 1280×720 @ 25 fps
- Supports 8-bit sensor parallel interface
- Supports dynamic frame rate data reception for BT.656/BT.1120
- Supports YUV422 data reception in multiple byte orders (e.g., Y1UY2V, Y1VY2U, Y2UY1V, and five other arrangements)
- Supports YUV to YCrCb data conversion
- Supports BT.656/BT.1120 blanking data reception in both EAV-first and SAV-first formats

2.5.12. DUAL_ORG

The TXW828-E016FL integrates one DUAL_ORG dual-lens processing module for dual-lens synchronization and data routing to the ISP. Key features are as follows:

- Supports dual-channel 1920×1080 @ 15 fps
- Supports dual-channel 1920×1080 and 1280×720 @ 25 fps
- Supports dual-channel 1280×720 @ 30 fps
- Supports DVP0, MIPI_CSI0, and MIPI_CSI1 as input sources
- Supports RAW8/10/12 and YUV422 data formats
- Supports adjustable output timing to ISP
- Supports FSYNC output for dual-lens synchronization control
- Supports data-save-only mode and software-triggered readback

2.5.13. GEN420

The TXW828-E016FL integrates one GEN420 module for converting external frame YUV420P data to the encoder. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports 8-bit pixel depth with YUV420P data source

2.5.14. GEN422

The TXW828-E016FL integrates one GEN422 module for converting external frame YUV420P data to YUV422 data. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports 8-bit pixel depth with YUV420P data source
- Supports conversion of PSRAM frame YUV420P data to YUV422 data
- Supports YUV output byte order adjustment
- Supports YUV output timing adjustment

- Supports output to PARA_OUT, VPP, and IMAGE_ISP
- Supports maximum resolution of 4000×4000

2.5.15. VPP Image Processing Module

The TXW828-E016FL integrates one VPP module for video data post-processing. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 40 fps
- Supports DVP0, MIPI_CSI0, MIPI_CSI1, IMAGE_ISP, GEN422, and PARA_IN as input sources
- Supports YUV422, RAW8/10/12, and RGB565/888S data formats; RAW and RGB formats support frame save only
- Supports YUV data byte order adjustment
- Supports YUV data range clipping
- Supports original data BUF0 and original/scaled data BUF1
- Supports proportional scaling for BUF1: 1/2, 1/3, 1/4, 1/6, and 2/3
- Supports Y-data-only mode for BUF0/1
- Supports solid color pattern and timestamp watermark
- Supports color border frame, motion detection, hardware-accelerated optical flow algorithm, and snapshot acceleration
- Supports Scatter DMA (YUV format only)

2.5.16. PRC Data Processing Module

The TXW828-E016FL integrates one PRC module for image data reordering. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports reordering of 16-line YUV422 data to YUV420P
- Supports YUV input byte order adjustment
- Supports Scatter DMA

2.5.17. H.264 Codec

The TXW828-E016FL integrates one H.264 video codec for image and video compression/decompression. Key features are as follows:

- Supports maximum resolution of 1920×1080 @ 30 fps
- Supports I-frames and P-frames
- Supports CBR, VBR, FIXQP, and QPMP bitrate control modes
- Supports encoding for 4 Regions of Interest (ROI)

2.5.18. MJPEG Codec

The TXW828-E016FL integrates one MJPEG video encoder and one MJPEG video codec for image and video compression/decompression. Key features are as follows:

- Supports maximum resolutions:
  - 8000×8000 @ 2 fps (snapshot mode)
  - 4000×4000 @ 5 fps (snapshot mode)
  - 1920×1080 @ 45fps;
  - 1280×720 @ 60fps;
  - 640×480 @ 120fps;
- Supports JPEG0/1 encoding with YUV420 pixel data format
- Supports JPEG1 decoding with YUV420/422/444 pixel data format
- Supports compressed data dual-buffer
- Supports dynamic quantization table (DQT) adjustment
- Supports JPEG header encoding/decoding
- Supports Gather DMA

2.5.19. LCD

The TXW828-E016FL integrates one LCD display interface controller and a

video post-processing hardware module. Key features are as follows:

- Supports RGB, MCU (8080 & 6800), SPI, QSPI, and MIPI DSI interfaces
- Supports image scaling, 90°/180°/270° rotation, and horizontal/vertical mirroring
- Supports image OSD and alpha blending
- Supports CCM, gamma correction, saturation, and contrast adjustment
- Supports dithering
- Supports screen recording
- RGB display output supports up to 1280×720 @ 60 fps

2.5.20. Ethernet MAC Controller

The TXW828-E016FL integrates one MAC module for wired Ethernet connectivity. Key features are as follows:

- Supports 10/100 Mbps
- Supports RMII and RGMII interfaces
- Supports half-duplex and full-duplex modes
- Supports up to 16 MAC address filters
- Supports ring descriptor structure
- Compliant with IEEE 802.3 CSMA/CD standard

2.5.21. SD Host Controller

The TXW828-E016FL integrates two SD host controllers supporting SD 1/4-bit mode with a maximum clock frequency of 50 MHz, for use with external SD cards or SDIO device interface peripherals.

2.5.22. M2M DMA Module

The TXW828-E016FL integrates three memory-to-memory (M2M) DMA controllers. These support DMA data transfers between SRAM-to-SRAM,

PSRAM-to-PSRAM, SRAM-to-PSRAM, and PSRAM-to-SRAM; M2M DMA0 additionally supports Flash-to-SRAM and Flash-to-PSRAM transfers. Key features are as follows:

- Supports byte alignment
- Supports up to 1 MB per transfer
- Supports memcpy and memset modes
- Supports 4-word cache buffer
- Supports transfer completion flag and interrupt

2.5.23. ISP

The TXW828-E016FL integrates a dedicated Image Signal Processor (ISP) that accepts RAW or YCbCr data for image processing. Key features are as follows:

- Supports YCbCr422 and RAW8/10/12 formats
- Supports images up to 1920×1080
- Supports image test mode
- Supports Black Level Correction (BLC)
- Supports Lens Shading Correction (LSC)
- Supports static/dynamic Defective Pixel Correction (DPC)
- Supports 2D and 3D noise reduction
- Supports digital gain
- Supports Green Imbalance Correction (GIC)
- Supports demosaicing interpolation
- Supports 3A algorithms: AWB, AE, and AF
- Supports Color Correction Matrix (CCM)
- Supports image dehazing
- Supports Gamma Correction
- Supports luma/chroma noise reduction (Y/CbCr domain)

- Supports image sharpening
- Supports adjustable image brightness, contrast, and saturation
- Supports image color detail adjustment including skin tone correction, color suppression, color enhancement, and chroma/saturation adjustment
- Supports motion detection
- Supports thermal imaging luminance colorization
- Supports multiple output formats: YUV444, YUV422, RGB565, and RGB888

2.5.24. MIPI DSI HOST

The TXW828-E016FL integrates one MIPI DSI HOST interface module. Key features are as follows:

- Supports maximum resolution of 1920×1080
- Supports transmission of all DSI packets via the APB interface
- Supports command transmission in low-speed and high-speed modes
- Supports up to 960 Mbps per data lane
- Supports up to 2 data lanes
- Data lane 0 supports bidirectional communication and escape mode
- Supports Ultra-Low Power (ULP) mode
- Supports ECC and checksum
- Supports End of Transmission Packet (EoTp)
- Supports error recovery mechanism
- Supports DPI and EDPI interfaces
- Supports video pattern generator: horizontal and vertical color bar generators
- Supports automatic ULPS control scheme
- Supports Tear effect request by hardware;
- Supports CSI transmission:

- Supports transmission of arbitrary CSI packets via the APB interface
- Supports transmission of ISP/GEN422 output images via the CSI protocol

2.5.25. Graphics Hardware Acceleration Modules

The TXW828-E016FL integrates dedicated graphics hardware acceleration modules to improve graphics processing performance. The modules are as follows:

2.5.25.1. DMA2D

The TXW828-E016FL integrates a DMA2D module, a dedicated DMA engine for image processing. Key features are as follows:

- Supports blending operations with up to 2 sources
- Alpha value is configurable (source value, fixed value, or modulated value)
- Supports up to 11 color formats with indirect or direct color encoding, from 4 bits per pixel up to 32 bits per pixel
- Uses 2 internal memories to store CLUTs in indirect color mode
- Supports 6 operating modes: register-to-memory, memory-to-memory, memory-to-memory with pixel format conversion, memory-to-memory with pixel format conversion and blending, fixed foreground blending, and fixed background blending
- Supports R/B channel swap and A channel inversion during pixel format conversion
- Supports abort and suspend of DMA2D operations
- Supports watermark interrupt generation when transferring a user-programmable target line
- Supports interrupt generation on bus error or access conflict
- Supports interrupt generation on transfer completion

In indexed or direct color mode, supports all standard color encoding schemes

from 4 bits per pixel up to 32 bits per pixel; DMA2D has a dedicated CLUT (Color Look-Up Table) memory.

2.5.25.2. LVGL Acceleration Module

The TXW828-E016FL integrates a partial LVGL acceleration module dedicated to accelerating time-consuming LVGL operations. Key features are as follows:

- Supports LVGL shadow acceleration functions: draw_corner_buf() and draw_mask_radius()
- Supports image fill
- Supports image transparency and color blending operations
- Supports image rotation
- Supports palette operation acceleration functions
- Supports graphics OSD

2.6. Timer Resources

2.6.1. Normal Timer

The TXW828-E016FL integrates four normal timers: timer0/3 are 32-bit timers, and timer1/2 are 16-bit timers with DMA and IR functions.

The following description uses 16-bit timer1 as an example; for timer0/3, all bit-width definitions are 32-bit accordingly.

Timer1 consists of a 16-bit auto-reload counter capable of measuring input signal pulse width (input capture) or generating output waveforms (output compare, PWM, etc.). Key features:

- 16-bit up-counter
- Programmable prescaler (modifiable in real time), supporting up to 128× division
- Supports GPIO as the count clock source
- Supports multiple count clock sources

- Allows update of the timer period register after each counter cycle
- Supports input capture function:
  - Supports saving up to 1 capture event pointer simultaneously
  - Each capture event polarity is independently configurable
  - Configurable counter reset on each capture event
- PWM output
- Supports auto-reload of period and duty cycle
- Supports synchronization circuit using external signals for timer control and timer
- Supports IR function

2.6.2. Simple Timer

The TXW828-E016FL integrates one simple timer module consisting of six 32-bit basic timers: stimer0 through stimer5. It supports multiple count clock sources and multiple operating modes including timer mode, counter mode, capture mode, and PWM mode.

2.6.3. Watchdog Timer

The TXW828-E016FL integrates two watchdog modules that operate independently of the system; CPU0 uses watchdog 0 and CPU1 uses watchdog 1. The watchdogs trigger a system reset to recover from abnormal conditions. The watchdog module operates on a clock derived from the always-on 64 kHz low-speed RC oscillator divided by 2, resulting in a 32 kHz clock independent of the system clock. The default configuration triggers a system reset every 2 seconds. Therefore, the user application must service the watchdog (feed the watchdog) before the reset occurs to restart the count. The watchdog reset interval is user-configurable in the range of 8 ms to 256 s. The operating mode can be configured to generate an interrupt or trigger a direct system reset. (Watchdog 1 is only operational when CPU1 is enabled; it is disabled by default.)

2.6.4. Always-On Domain Timers

The TXW828-E016FL always-on power domain integrates the following 7 timers, used as wake-up sources in low-power mode, PWM output in low-power mode, and timekeeping in low-power mode:

- 1× always-on domain 32-bit timer PD_CORE_AOTIMER (supports low-power mode wake-up)
- 1× always-on domain 31-bit timer PD_CORE_TIMER (supports low-power mode wake-up; can be powered off in the lowest power mode)
- 4× 16-bit LED timers supporting PWM output from designated I/Os in low-power mode
- 1× 64-bit read-only counter that starts counting from power-on, cannot be cleared, and its current value is readable by software

2.7. Security Hardware Accelerators

2.7.1. CRC Module

The TXW828-E016FL integrates one CRC module for data verification. Key features are as follows:

- Supports polynomials of various lengths: 5/7/8/16/32 bits
- Supports user-defined polynomials
- Supports CRC verification of multiple segmented data blocks

2.7.2. AES Module

The TXW828-E016FL integrates one AES module for data encryption and decryption. Key features are as follows:

- Supports AES-128/192/256 encryption and decryption in ECB, CBC, and CTR modes
- Supports DMA mode; maximum DMA data length of 1 MB

2.7.3. SHA Module

The TXW828-E016FL integrates one SHA module for data verification. Key features are as follows:

- Supports SHA-1 and SHA2-256
- Supports DMA mode; maximum DMA data length of 65536 bytes
- Supports SHA computation on multiple segmented data blocks
- Maximum data rate: 560 Mbps @ 192 MHz (system clock)

2.7.4. TRNG Module

The TXW828-E016FL integrates one True Random Number Generator (TRNG) module for secure random seed generation.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{VCC}	Operating voltage	-	-0.3	3.6	V
V_{VCCA}	Analog supply voltage	-	-0.3	3.6	V
$VCCPA$ $VCCRF$	RF supply voltage	-	-0.3	3.6	V
T_{ST}	Storage temperature	-	-40	150	°C

Operation beyond the absolute maximum ratings may cause permanent damage to the device. Operation outside the recommended operating conditions but within the absolute maximum ratings may affect device reliability, functionality, and performance, and may shorten device lifetime.

3.2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{VCC}	Operating voltage	-	3	3.3	3.6	V
V_{VCCA}	Analog supply voltage	-	3	3.3	3.6	V
$VCCPA$ $VCCRF$	RF supply voltage	-	3	3.3	3.6	V
$VCAM^{(1)}$	VCAM LDO load capacity	OC=0, VCAM = 2.8V	-	-	100	mA
$VCC18$	VCC18 LDO load capacity	OC=3, VCC18 = 1.8V	-	-	100	mA
$VCAM2$	VCAM2 LDO load capacity	OC=3, VCC12 = 1.2V	-	-	100	mA
T_A	Operating temperature	-	-40	-	85	°C

(1) The VCAM/VCC18 LDO load capacity specifications apply at an operating temperature of 85°C. VCAM LDO load capacity increases as temperature decreases; decreases as VCC voltage decreases; and increases as the VCAM voltage level decreases.

Notes:

1. At 25°C, the PSRAM itself consumes approximately 50 mA of the VCC18 LDO load capacity.

3.3. DC Electrical Characteristics (3.3 V, 25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.
CIN	Pin capacitance	-	2	-	pF
VIH	High-level input voltage	0.6*VCCIO	-	VCCIO+0.3	V
VIL	Low-level input voltage	-0.3	-	0.4*VCCIO	V
IIH	High-level input current	-	-	50	nA
IIL	Low-level input current	-	-	50	nA
VOH	High-level output voltage	0.9*VCCIO	-	-	V
VOL2	Low-level output voltage	-	-	0.1*VCCIO	V
IOH	Source current, high level (VCC = 3.3 V, VOH >= 2.64 V,PAD_DRIVER = 3)	-	20	-	mA
IOL	Sink current, low level (VDD1 = 3.3 V, VOL = 0.5 V,PAD_DRIVER = 3)	-	96	-	mA
RPU	Pull-up resistance	4.7	100	100	kΩ
RPD	Pull-down resistance		100		kΩ
VIH_nRST	MCLR reset release voltage	0.6*VCCIO	-	VCCIO+0.3	V
VIL_nRST	MCLR reset voltage	-0.3	-	0.4*VCCIO	V

Notes:

1. VOH and VOL are measured under high-impedance load conditions.

2. VCCIO refers to the power supply voltage of the corresponding GPIO.

3.4. AC Electrical Characteristics

3.4.1. External Clock Source Characteristic

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{xoscm}	User external clock frequency			40		MHz
V_{BIAS}	XOSCI/XOSCO bias level	-	-	550	-	mV
V_{xoh}	XOSCI input pin high-level voltage	-	-	0.77	-	V
V_{xol}	XOSCO input pin low-level voltage	-	-	0.33	-	V
$Duty_{(xoscm)}$	Duty cycle	-	42	-	58	%
ACC_{xoscm}	HSE accuracy	-	-	-	-	ppm
$t_{SU(xoscm)}$	Start-up time	-	-	5		ms
$I_{VCCA(XOSCM)}$	XOSCM oscillator power consumption	Average current consumption	-	0.7	-	mA

3.4.2. Internal Clock Source Characteristics

Table 3-4-2-1: RC8M Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{VCCA}	Supply voltage	-	3	3.3	3.6	V
RC8M	Frequency	25°C	6	8	10	MHz
ACC_{RC8M} (3)	RC8M oscillator accuracy	-40°C to +85°C	-38	-	+25	%
$t_{SU(RC8M)}$	RC8M oscillator start-up time	-	-	60	-	us
$I_{VCCA(RC8M)}$	RC8M oscillator power consumption	Average current consumption	-	10	-	uA

Table 3-4-2-2: RC128K Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RC128K	Frequency	TA=25°C	-	128	-	kHz
$I_{DD(RC128K)}$	RC128K oscillator power consumption	-	-	10	-	uA

3.5. Power Consumption Characteristics

3.5.1. RF Power Consumption

The following power consumption data are measured at VCC_RF/PA and VCC15L/R/O under a 3.3 V supply at 25°C ambient temperature. All TX data are measured at 100% duty cycle.

RF Power Consumption (measured at 100% duty cycle)			
Operating Mode	**Description**		**Average (mA)**
Active	TX	802.11g, 20 MHz, 54 Mbps, 14dBm	254
		802.11n, 20 MHz, MCS7, 14dBm	254
	RX	802.11b/g/n, 20 MHz	38

The following power consumption data are estimated:

RF Power Consumption (estimated at 50% duty cycle)			
Operating Mode	**Description**		**Average (mA)**
Active	TX+RX	802.11g, 20 MHz, 54 Mbps, 14dBm	146
		802.11n, 20 MHz, MCS7, 14dBm	146

3.5.2. CPU Power Consumption

MCU State	WLAN State	RTC	Test Condition		Power Consumption
$LP^{(1)}$	OFF	ON	Always-on power domain logic active; all SRAM powered; VCC/VDD supplied via DCDC with 5 V input	-	11.88uA
$ULP^{(1)}$	OFF	ON	Always-on power domain logic active; 16 KB SRAM powered; VCC/VDD supplied via DCDC with 5 V input	-	4.43uA

(1) Supports wake-up via I/O, timer, and WDT

3.5.3. System Sleep Keep-Alive Power Consumption

Notes:

The following power consumption data are measured under a shielded environment at 3.6 V VCC, 1.05 V VDD (DCDC), 25 °C ambient temperature, and a 1 ms STA RX beacon window.

Test Condition	DTIM1 (uA)	DTIM3 (uA)	DTIM5 (uA)	DTIM6 (uA)	DTIM10 (uA)	DTIM30 (uA)
External 32K	1091	427	301	269	214	176
Internal 32K	1085	418	285	252	185	118

Notes:

1) When using the internal 32K crystal oscillator, longer sleep durations introduce greater timing error, which may result in increased power consumption.
2) Wi-Fi PS mode power consumption increases in interference environments; results may vary across different interference conditions.

3.6. Reliability

3.6.1. ESD Electrical Characteristics

Symbol	Parameter	Test Condition	Max.	Unit	Class
ESD	Electrostatic discharge Human Body Model (HBM)	TA = + 25°C, JEDEC EIA/JESD22-A114	2000	V	-
	Electrostatic discharge, Charged Device Model (CDM)	TA = + 25°C, JEDEC EIA/JESD22-C101-B	1000	V	-

3.6.2. Latch-Up Electrical Characteristics

Symbol	Parameter	Test Condition	Max.	Unit	Class
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (TA = +25 °C)	±200	mA

3.7. Wi-Fi RF Performance and Power Consumption

3.7.1. Wi-Fi Transmitter Performance

Parameter	Condition	Typ. (dBm)
Output power	802.11g, 20 MHz, 54 Mbps	14
	802.11n, 20 MHz, MCS7	14
	802.11n, 20 MHz, MCS0	19

3.7.2. Wi-Fi Receiver Performance

Parameter	Condition	Typ. (dBm)
Receiver sensitivity	HT20 MCS7 4k	-72
	NONHT 54M	-74
	NONHT 6M	-90
	CCK11M	-86
	CCK5.5M	-89
	DSSS2M	-91
	DSSS1M	-96

3.7.3. BLE Transmitter Performance

Parameter	Condition	Typ. (dBm)
Output power		20

3.7.4. BLE Receiver Performance

Parameter	Condition	Typ. (dBm)
Receiver sensitivity	1Mbps	-94.5

3.8. Audio Performance

3.8.1. Audio ADC Performance

Parameter	Condition	Typ. (dB)
SNR	1 kHz sine wave, sample rate = 44.1 kHz, bit rate = 44.1×16 kbps, A-weighting	89
THD+N	1 kHz sine wave, sample rate = 44.1 kHz, bit rate = 44.1×16 kbps, A-weighting	-78

3.8.2. Audio DAC Performance

Parameter	Condition	Typ. (dB)
SNR	1 kHz sine wave, sample rate = 44.1 kHz, bit rate = 44.1×16 kbps, A-weighting	88
THD+N	1 kHz sine wave, sample rate = 44.1 kHz, bit rate = 44.1×16 kbps, A-weighting	-78

4. Reference Design

5. Ordering Information

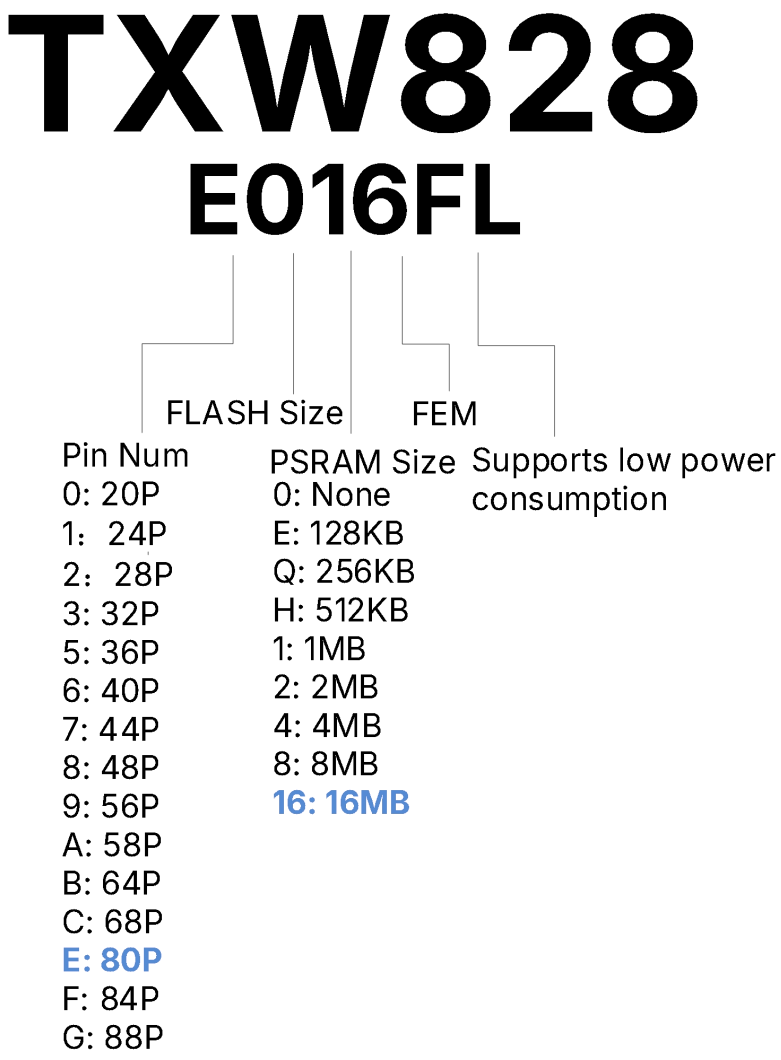


Figure 5-1: TXW828-E016FL Part Number Nomenclature

Table 5-1: Ordering Information

Part Number	Package	Size	Description
TXW828-E016FL	QFN80	8x8	Built-in 16 MB PSRAM; supports Wi-Fi low-power Audio & Video applications with display output